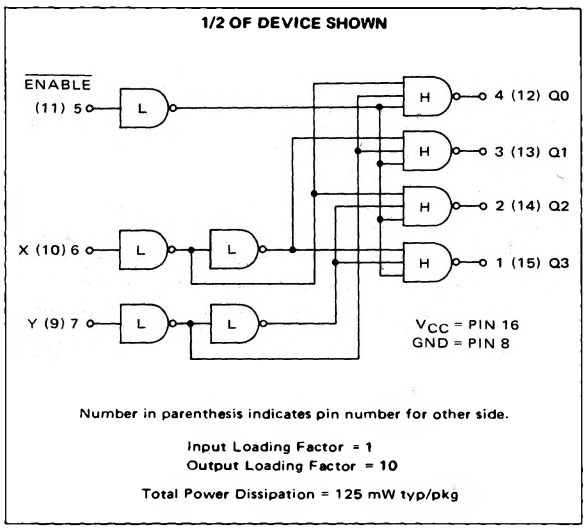
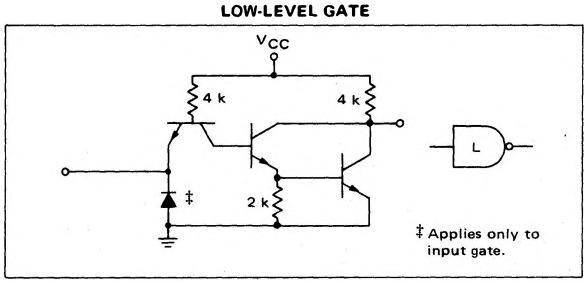
DUAL BINARY TO
ONE-OF-FOUR LINE DECODER

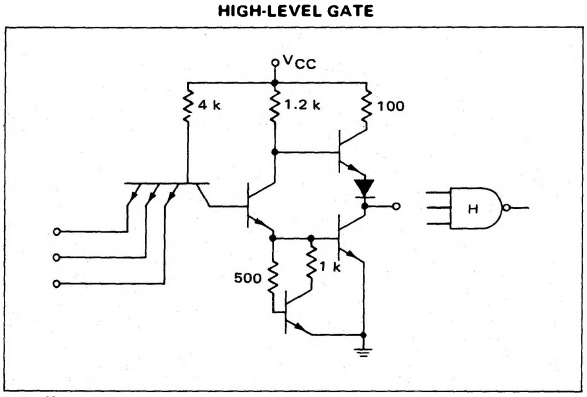
MC4007L,P*



LOW-LEVEL GATE



HIGH-LEVEL GATE



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin in-line plastic package (Case 612).

This device converts two lines of input data to a one-of-four output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The dual 2-input/4-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

TRUTH TABLE

E = 0

X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
0 = Low State

TYPICAL TURN-ON DELAY TIMES (ns)
$T_A = 25^oC$

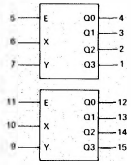
Input	Q0	Q1	Q2	Q3
X	11.5	15.5	11.5	15.5
Y	11.5	11.5	15.5	15.5
$\overline{E}$	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
$T_A = 25^oC$

Input	Q0	Q1	Q2	Q3
X	14.0	19.0	14.0	19.0
Y	14.0	14.0	19.0	19.0
$\overline{E}$	14.5	14.5	14.5	14.5

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner. Additionally, test all input-output combinations according to the truth table.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	17.6	16	-1.6	1.0	-	1.1	2.0	0.4	2.5	4.5	-	5.0	4.75	5.25
+25°C	17.6	16	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.5	7.0	5.0	4.75	5.25
+75°C	17.6	16	-1.6	1.0	-	0.9	1.8	0.4	2.5	4.5	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4007 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																								
Forward Current	I_{F1}	5	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	16	8
Leakage Current	I_R	5	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	16	8
Breakdown Voltage	BV_{in}	5	-	-	5.5	-	-	-	Vdc	-	-	-	5	-	-	-	-	-	-	-	-	-	16	8
Clamp Voltage	V_D	5	-	-	-	-1.5	-	-	Vdc	-	-	-	-	5	-	-	-	-	-	-	-	16	-	8
Output																								
Output Voltage	V_{OL1}	4	-	0.4	-	0.4	-	0.4	Vdc	4	-	-	-	-	5,6,7	-	-	-	-	-	-	16	-	8
	V_{OL2}	4	-	0.4	-	0.4	-	0.4	Vdc	-	4	-	-	-	5,6,7	-	-	-	-	-	-	16	-	8
	V_{OH}	4	2.5	-	2.5	-	2.5	-	Vdc	-	-	4	-	-	5,6	7	-	-	-	-	-	16	-	8
Short-Circuit Current	I_{SC}	4	-20	-60	-20	-60	-20	-60	mAdc	-	-	-	-	-	-	-	-	-	5	-	16	-	-	4,8
Power Requirements (Total Device)																								
Maximum Power Supply Current	I_{max}	16	-	-	-	51	-	-	mAdc	-	-	-	-	-	-	-	-	-	5,6,7,9,10,11	16	-	-	-	8
Power Supply Drain	I_{PD}	16	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	5,11	-	6,7,9,10	-	16	-	-	8

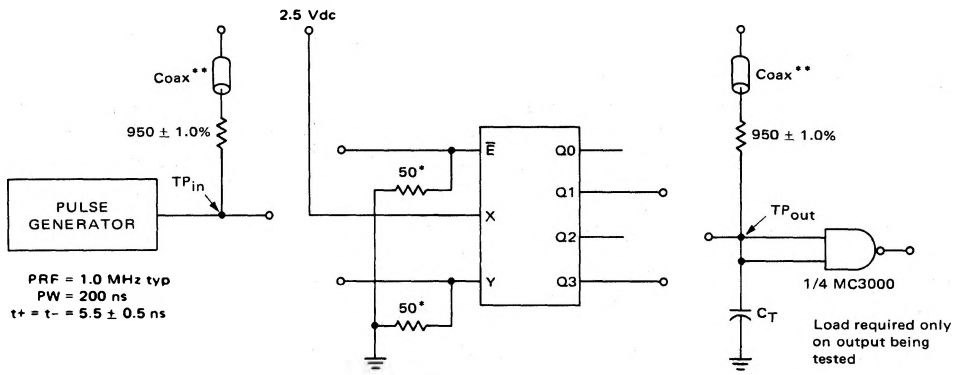
INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15[*,*]	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

[*,*] Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT



*Resistor used only on input under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	Ē	Y	Q1	Q3	LIMITS Max	LIMITS Unit
t_{pd+} (Y to Q1)	Gnd	A	C	–	20	ns
t_{pd-} (Y to Q1)	Gnd	A	C	–	17	ns
t_{pd+} (Y to Q3)	Gnd	A	–	B	29	ns
t_{pd-} (Y to Q3)	Gnd	A	–	B	23	ns
t_{pd+} (Ē to Q3)	A	2.5 V	–	C	21	ns
t_{pd-} (Ē to Q3)	A	2.5 V	–	C	20	ns

VOLTAGE WAVEFORMS