## MC4010L, $\mathbf{P}$ *



## ADVANCE INFORMATION/NEW PRODUCT

Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic " 1 " states on the inputs will result in a logic " 1 " output state. An odd parity checker can be made by connecting an inverter to the output of the device.

This function is constructed using low and high-level Exclusive NOR gates connected as shown in the logic diagram to maximize output drive capability and minimize power dissipation.


LOW-LEVEL GATE


[^0]MC4010L, P (continued)

INPUT and OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

|  | MC4000 <br> INPUT | MC4000 <br> OUTPUT |
| :--- | :---: | :---: |
| FAMILY | LOADING | LOADING |
| FACTOR | FACTOR |  |
| MC4000 | 1.0 | 10 |
| MC400 | 1.0 | 10 |
| MC2000 | 0.67 | 6 |
| MC3000 | 0.7 | 8 |
| MC7400 | 1.0 | 10 |
| MC830 | $1.15^{* *}$ | 12 |

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.
**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic " 1 " state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS
( $T_{A}=0$ to $75^{\circ} \mathrm{C}$ )

| Characteristic | Symbol | Value | Conditions |
| :---: | :---: | :---: | :---: |
| Input |  |  |  |
| Forward Current | IF1 | -3.2 mAdc max | $\mathrm{V}_{\text {in }}=0.4 \mathrm{Vdc}, \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{Vdc}$ |
|  | 'F2 | -2.8 mAdc max | $\mathrm{V}_{\text {in }}=0.4 \mathrm{Vdc}, \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{Vdc}$ |
| Leakage Current | ${ }^{1} \mathrm{R}$ | $80 \mu$ Adc max | $\mathrm{V}_{\text {in }}=2.5 \mathrm{Vdc}, \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{Vdc}$ |
| Breakdown Voltage | $B V_{\text {in }}$ | 5.5 Vdc max | $\mathrm{I}_{\text {in }}=1.0 \mathrm{mAdc}, \mathrm{V}_{\text {CC }}=5.25 \mathrm{Vdc}, \mathrm{T}_{A}=25^{\circ} \mathrm{C}$ |
| Clamp Voltage | $V_{\text {D }}$ | -1.5 Vdc max | ${ }^{1} \mathrm{D}=-10 \mathrm{mAdc}, \mathrm{V}_{C C}=4.75 \mathrm{Vdc}, \mathrm{T}_{A}=25^{\circ} \mathrm{C}$ |
| Threshold Voltage | $V_{\text {th " }}$ " ${ }^{\text {r }}$ | 2.0 Vdc <br> 1.8 Vdc | $\begin{aligned} & T_{A}=0^{\circ} \mathrm{C} \\ & T_{A}=+25^{\circ} \mathrm{C}, \text { or } T_{A}=+75^{\circ} \mathrm{C} \end{aligned}$ |
|  | $V_{\text {th }}$ "0" | 1.1 Vdc 0.9 Vdc | $\begin{aligned} & T_{A}=0^{\circ} \mathrm{C}, \text { or } T_{A}=+25^{\circ} \mathrm{C} \\ & T_{A}=+75^{\circ} \mathrm{C} \end{aligned}$ |
| Output Output Voltage | $\mathrm{V}_{\mathrm{OL}}$ | 0.4 Vdc max <br> 0.4 Vdc max | $\begin{aligned} & \mathrm{I}_{\mathrm{OL}}=16 \mathrm{mAdc}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{Vdc}^{\dagger} \\ & \mathrm{I}_{\mathrm{OL}}=17.6 \mathrm{mAdc}, \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{Vdc}{ }^{\dagger} \end{aligned}$ |
|  | $\mathrm{V}_{\mathrm{OH}}$ | 2.5 Vdc min | ${ }^{1} \mathrm{OH}=-1.6 \mathrm{mAdc}, \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{Vdct}$ |
| Short-Circuit Current | ISC | -20 to -65 mAdc | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{Vdc}$, output grounded $\dagger$ |

TThese tests are performed according to the logic equations with a true input equal to $\mathrm{V}_{\text {th }}$ " 1 " and a false input equal to $\mathrm{V}_{\text {th }}$ " 0 ".


[^0]:    - L suffix $=$ TO-116 ceramic dual in-line package (Case 632).
    $P$ suffix $=$ TO-116 plastic dual in-line package (Case 605).

