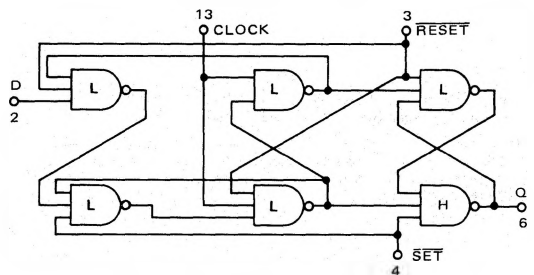


QUAD TYPE D FLIP-FLOP

MC4300/MC4000 series

MC4015L,P*

1/4 OF DEVICE SHOWN
(CLOCK AND RESET COMMON TO ALL FOUR FLIP-FLOPS)



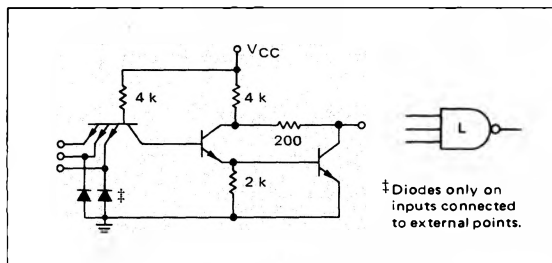
Input Loading Factor:
D = 1 CLOCK = 8
SET = 2 RESET = 8

Output Loading Factor = 10

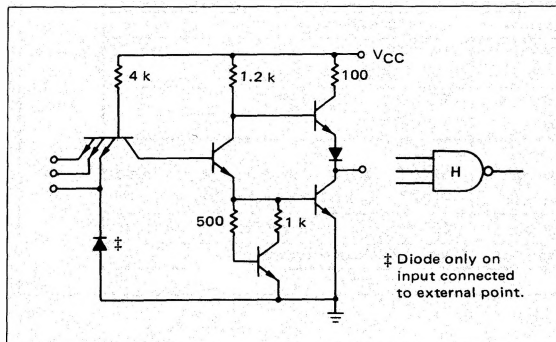
Total Power Dissipation = 190 mW typ/pkg
Propagation Delay Time = 16 ns typ
Setup Time = 10 ns max
Hold Time = 10 ns max
Operating Frequency = 30 MHz typ

VCC = PIN 16
GND = PIN 8

LOW-LEVEL GATE

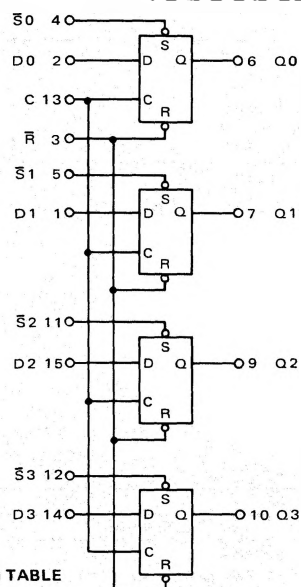


HIGH-LEVEL GATE



This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.



TRUTH TABLE

D	Q _{n-1}	Q _n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

OPERATING CHARACTERISTICS

Data must be present at the D input 10 ns prior to the rise of the clock, and remain 10 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (10 ns) and the hold time (10 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and \bar{Q} respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct Set or Reset inputs.

* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

MC4015L,P (continued)

INPUT and OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

FAMILY	MC4015 INPUT LOADING FACTOR	MC4015 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	12
MC830	1.15**	10

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — D SET RESET, CLOCK	I _{F1}	-1.6 mA dc max -3.2 mA dc max -12.8 mA dc max	V _{in} = 0.4 V dc, V _{CC} = 5.25 V dc
D SET RESET, CLOCK	I _{F2}	-1.4 mA dc max -2.8 mA dc max -11.2 mA dc max	V _{in} = 0.4 V dc, V _{CC} = 4.75 V dc
Leakage Current — D SET RESET, CLOCK	I _R	40 μA dc max 80 μA dc max 320 μA dc max	V _{in} = 2.5 V dc, V _{CC} = 5.25 V dc
Breakdown Voltage	BV _{in}	5.5 V dc max	I _{in} = 1.0 mA dc, V _{CC} = 5.25 V dc, T _A = 25°C
Clamp Voltage	V _D	-1.5 V dc max	I _D = -10 mA dc, V _{CC} = 4.75 V dc, T _A = 25°C
Threshold Voltage	V _{th} "1"	2.0 V dc	T _A = 0°C
		1.8 V dc	T _A = +25°C, or T _A = +75°C
	V _{th} "0"	1.1 V dc 0.9 V dc	T _A = 0°C, or T _A = +25°C T _A = +75°C
Output			
Output Voltage	V _{OL}	0.4 V dc max 0.4 V dc max	RESET = 0, I _{OL} = 16 mA dc, V _{CC} = 4.75 V dc RESET = 0, I _{OL} = 17.6 mA dc, V _{CC} = 5.25 V dc
		V _{OH}	2.5 V dc min SET = 0, I _{OH} = -1.6 mA dc, V _{CC} = 4.75 V dc
Short-Circuit Current	I _{SC}	-20 to -65 mA dc	V _{CC} = 5.0 V dc, output grounded