PROGRAMMABLE MODULO-N
DECADE COUNTER

MC4316L • MC4016L,P*

PROGRAMMABLE MODULO-N
HEXADECIMAL COUNTER

MC4318L • MC4018L,P*

ADVANCE INFORMATION/NEW PRODUCT

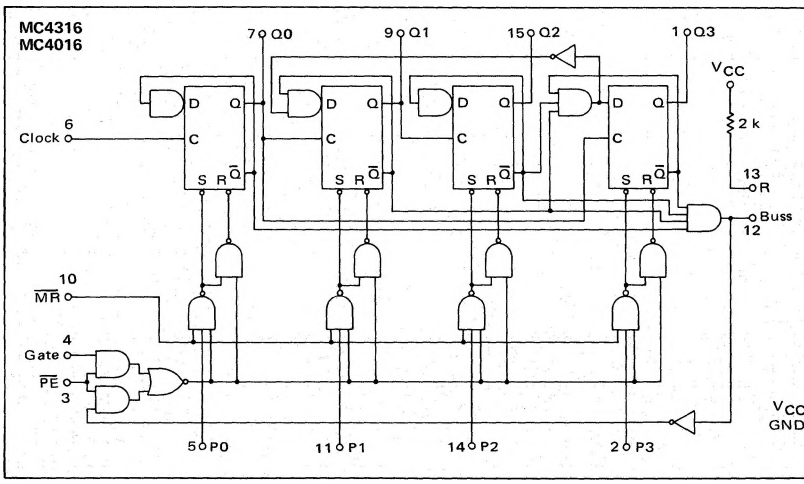
These devices are programmable, cascadable, modulo-N counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15.

The $\overline{PE}$ input enables the parallel preset inputs P0 thru P3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All preset inputs are independent of the logic level of the Clock.

The Gate input and Buss node are useful in cascading of counters. A 2.0 kilohm pullup resistor to be used with the Buss node is provided internally (pin 13).

When the counters are used in divide-by-N capacity, the Buss output provides a pulse of width equal to the clock pulse and at an interval determined by N.

Modulo-N counters are useful in frequency synthesizers, in phase-locked-loops, and in other applications where a simple method for frequency division is needed.

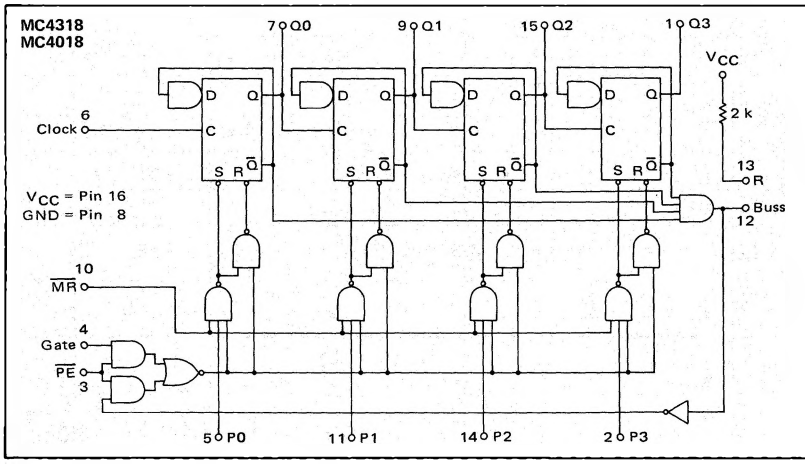


COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Both Types:

Input Loading Factor:
Clock, $\overline{PE}$ = 2
P0, P1, P2, P3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Buss = 35 ns typ

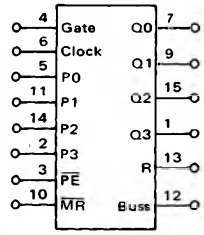


COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

*L suffix = 16-pin ceramic dual in-line package (Case 620).
P suffix = 16-pin plastic dual in-line package (Case 612).

ELECTRICAL CHARACTERISTICS

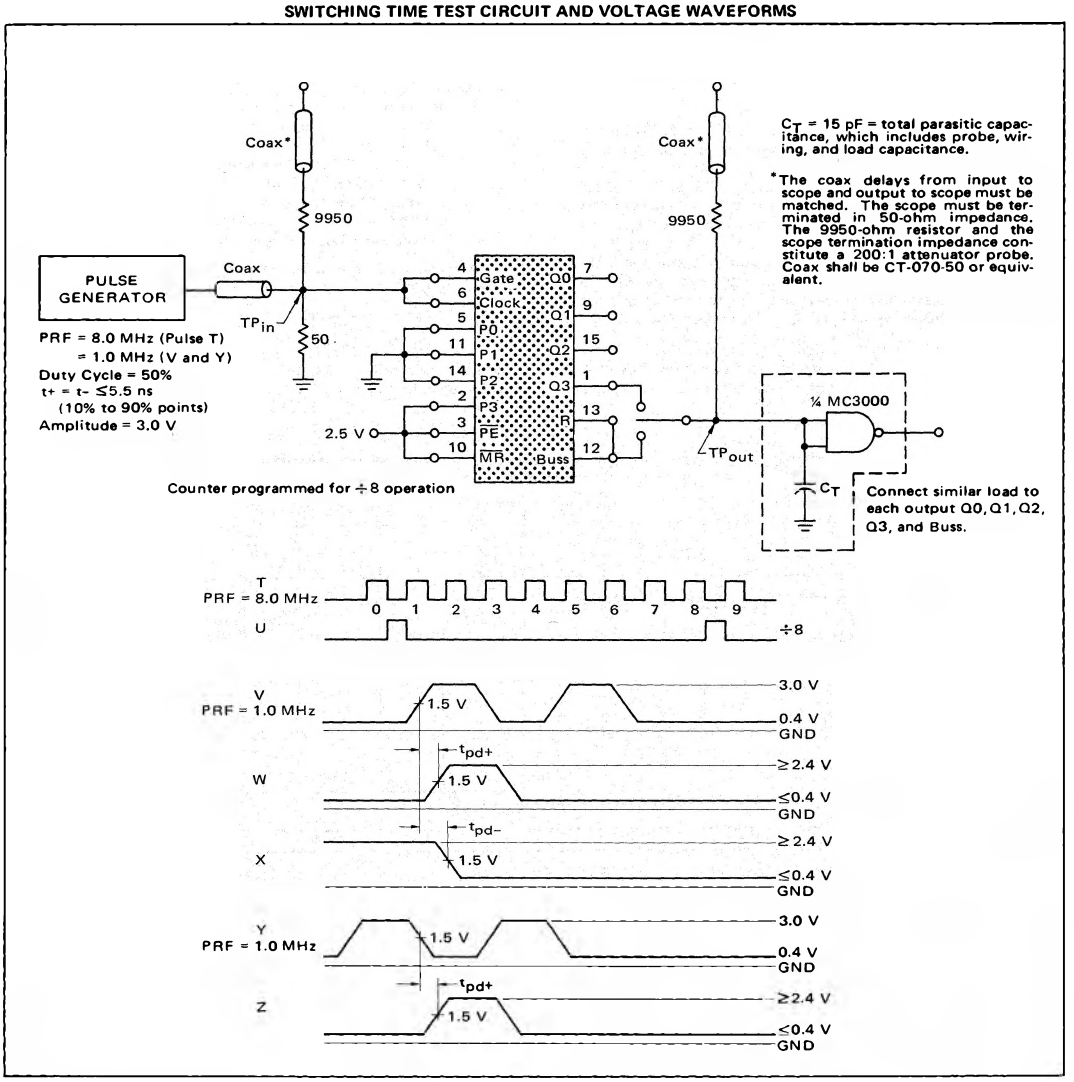
Tests are shown for one output only. Others are tested in the same manner.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{in}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC4316, MC4318	-55°C	12.8	13.8	9.6	-1.6	–	1.1	2.0	0.4	2.4	–	5.0	4.5	5.5
	+25°C	12.8	13.8	9.6	-1.8	1.0	1.1	1.8	0.4	2.4	8.0	5.0	4.5	5.5
	+125°C	12.8	13.8	9.6	-1.6	–	0.8	1.8	0.4	2.4	–	5.0	4.5	5.5
MC4016, MC4018	0°C	12.8	13.8	9.6	-1.6	–	1.1	2.0	0.4	2.5	–	5.0	4.75	5.25
	+25°C	12.8	13.8	9.6	-1.8	1.0	1.1	1.8	0.4	2.5	7.0	5.0	4.75	5.25
	+75°C	12.8	13.8	9.6	-1.6	–	0.9	1.8	0.4	2.5	–	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4316, MC4318 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4016, MC4018 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_{F1}	2	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	2	10	–	–	–	16	3,8
		3	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	–	–	3	4	–	–	–		8,12
		4	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	4	3	–	–	–		8
		5	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	5	10	–	–	–		3,8
		6	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	–	–	6	–	–	–	–		8
		10	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4		–	–	–	–	–	–	–	10	2,5,11,14	–	–	–		3,8
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	11	10	–	–	–		
		14	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	14	10	–	–	–		
	I_{F2}	2	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc	–	–	–	–	–	–	–	2	10	–	–	16	–	3,8
		3	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	–	–	3	4	–	–		–	8,12
		4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	4	3	–	–			8
		5	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	5	10	–	–		–	3,8
		6	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	–	–	6	–	–	–			8
		10	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6		–	–	–	–	–	–	–	10	2,5,11,14	–	–		–	3,8
		11	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	11	10	–	–		–	
		14	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	14	10	–	–		–	
Leakage Current	I_R	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	–	–	2	–	–	–	16	8,10
		3	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	–	–	3	–	–	–		4,8
		4	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	4	–	–	–		3,8
		5	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	5	–	–	–		8,10
		6	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	–	–	6	–	–	–		8
		10	–	160	–	160	–	160	–	160	–	160	–	160		–	–	–	–	–	–	–	–	10	–	–	–		2,5,8,11,14
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	11	–	–	–		8,10
		14	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	14	–	–	–		8,10
Breakdown Voltage	BV_{in}	2	5.5	–	5.5	–	5.6	–	5.5	–	5.5	–	5.5	–	Vdc	–	–	–	–	2	–	–	–	–	–	–	–	16	8,10
		3		–		–		–		–		–		–		–	–	–	–	3	–	–	–	–	–	–	–		4,8
		4		–		–		–		–		–		–		–	–	–	–	4	–	–	–	–	–	–	–		3,8
		5		–		–		–		–		–		–		–	–	–	–	5	–	–	–	–	–	–	–		8,10
		6		–		–		–		–		–		–		–	–	–	–	6	–	–	–	–	–	–	–		8
		10		–		–		–		–		–		–		–	–	–	–	10	–	–	–	–	–	–	–		2,5,8,11,14
		11		–		–		–		–		–		–		–	–	–	–	11	–	–	–	–	–	–	–		8,10
		14		–		–		–		–		–		–		–	–	–	–	14	–	–	–	–	–	–	–		8,10
Output																													
Output Voltage	V_{OL}	1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	1	–	–	–	–	2,3,5,11,14	–	–	–	–	–	–	16	–	8
		1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4		–	1	–	–	–	2,3,5,11,14	–	–	–	–	–	–	–	16	
		12	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5		–	–	12	–	–	3	2,5,11,14	–	–	–	–	–	16	–	
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	1	–	3	2,5,11,14	–	–	–	–	–	16	–	8
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	–	12	2,3,5,11,14	–	–	–	–	–	–	16	–	8
Short-Circuit Current	I_{SC}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	–	3	2,5,11,14	–	16	–	–	1,8
		13	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8,13
Power Requirements (Total Device)																													
Power Supply Drain	I_{PD}	16	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	P0, P1, P2 Pins 5,11,14	P3, $\overline{PE}$, $\overline{MR}$ Pins 2,3,10	Buss, R Pins 12,13	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{Tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Buss	t_{pd+}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Clock to Q3	t_{pd+}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
	t_{pd-}	V	V	Gnd	2.5 V	–	X	–	78	ns

OPERATING CHARACTERISTICS

Basic operation of the MC4316/4016 and MC4318/4018 is the same. When operated as single stages, the Gate and Clock inputs must be tied together. The internal pullup resistor must be connected to the Buss node (pin 13 to pin 12). The programmable counter is set to count down by a pre-determined number (N) before recycling, according to the binary code present at the parallel preset inputs, P0 thru P3 (see the truth table). The binary information at inputs P0 thru P3 is preset into the counter after applying a logic "0" to the $\overline{PE}$ input. Data may be entered synchronously or asynchronously while $\overline{PE}$ is low, or when outputs Q0, Q1, Q2 and Q3 are in the logic "0" state and the Clock is low.

The counters may be set to divide by 10 (MC4316/4016) or 16 (MC4318/4018) regardless of preset input states by applying a logic "0" to the Buss node. This, in effect, disables the preset inputs and causes a logic "0" to appear at the preset of each flip-flop of the counter. If a binary number greater than nine (1001) is applied to the preset inputs of the MC4316/4016, the counter will ignore the most significant bit and recognize only the three least significant bits.

Cascading of Counters

To cascade counters (Figure 1):

1. Connect Gate inputs of all stages to the Clock of the first stage.
2. Connect all Buss outputs to one common pullup resistor (2.0 kilohms, internal).
3. Connect the Clock input of each stage after the first stage to the Q3 output of the previous stage.
4. Take the divide-by-N pulse from the Buss outputs.

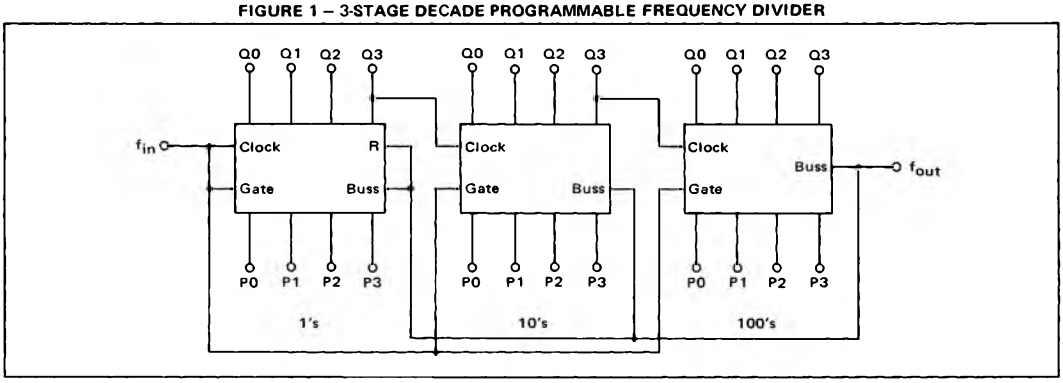
When cascaded, the count mode of the entire string of counters is defined by:

$$N = N_0 + 10\,N_1 + 100\,N_2 + \ldots \text{ (MC4316/4016)}$$

or $$N = N_0 + 16\,N_1 + 256\,N_2 + \ldots \text{ (MC4318/4018)}$$

where N_0, N_1, N_2, . . . are the BCD or binary numbers programmed at the zero, first, second, . . . stages.

FIGURE 1 – 3-STAGE DECADE PROGRAMMABLE FREQUENCY DIVIDER



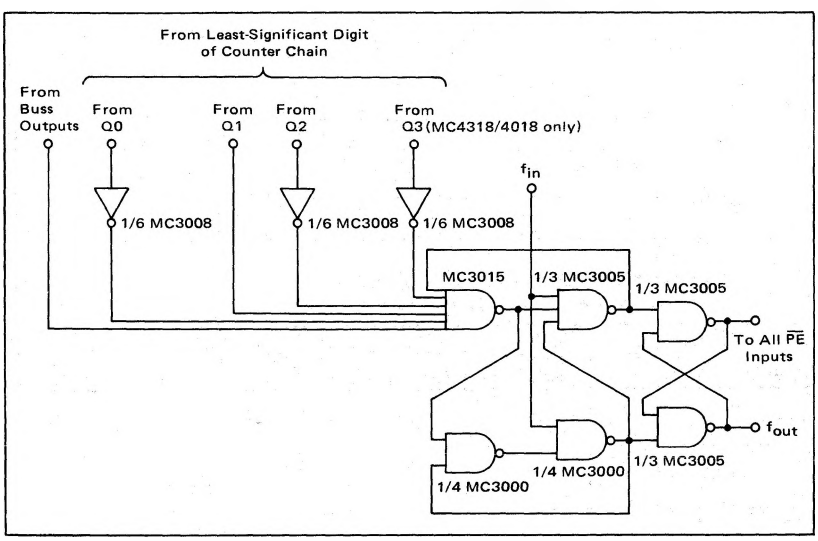


FIGURE 2 – FREQUENCY EXTENDER

APPLICATIONS INFORMATION

The maximum operating frequency of the MC4316/4016 or MC4318/4018 may be extended at the expense of decreased flexibility. By using the circuit shown in Figure 2 it is possible to extend the useful frequency (f_{tog}) of the counters to 25 MHz. It then becomes impossible to count by 0, 1, or 2. The output pulse width of the extended counter-chain is twice the width of the clock pulse.

Figure 3 shows the extended circuitry incorporated in a system of cascaded counters. The inverter shown connected by dotted lines is used only with the MC4318/4018.

FIGURE 3 – CASCADED PROGRAMMABLE COUNTER USING FREQUENCY EXTENDER

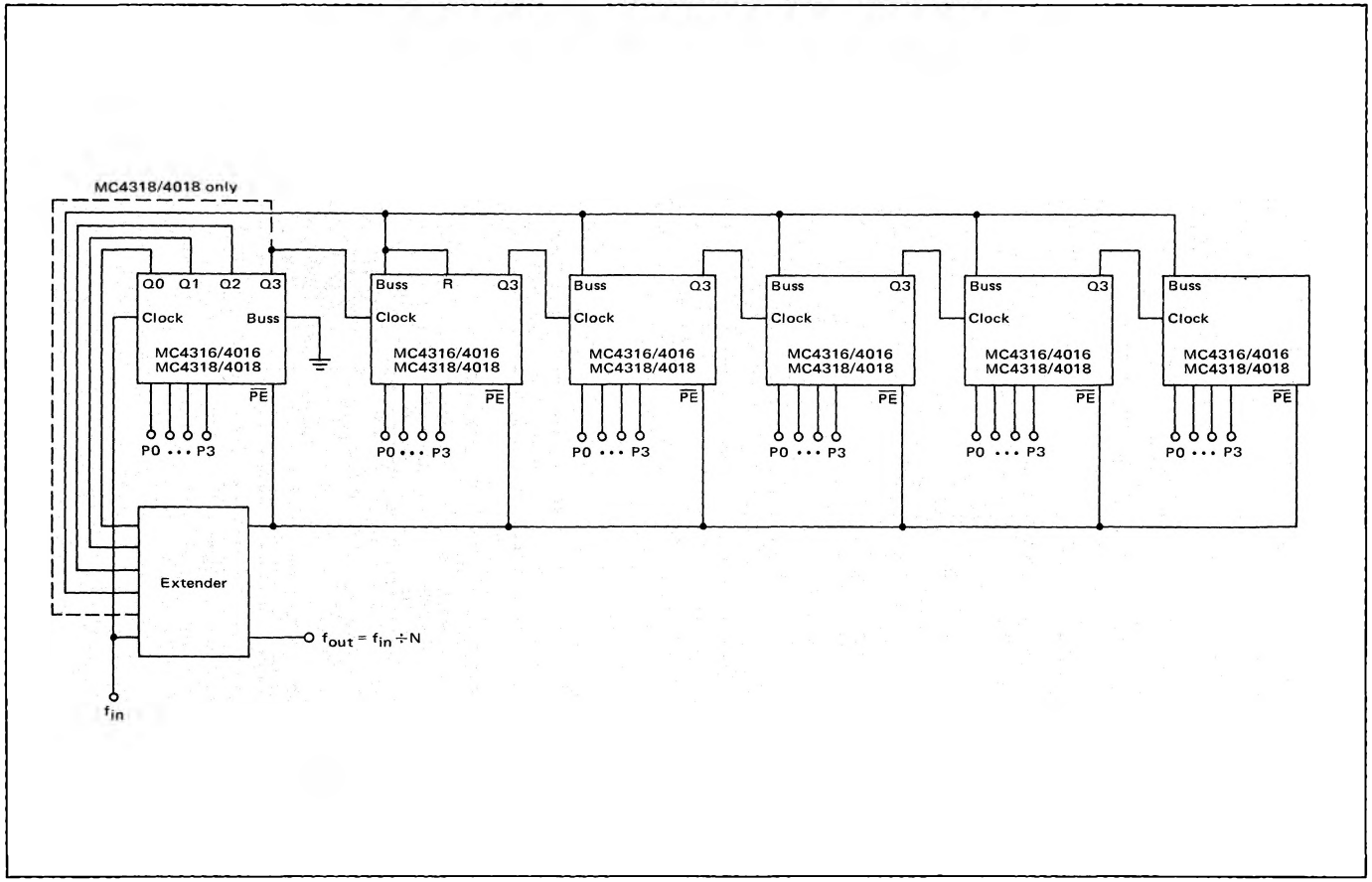
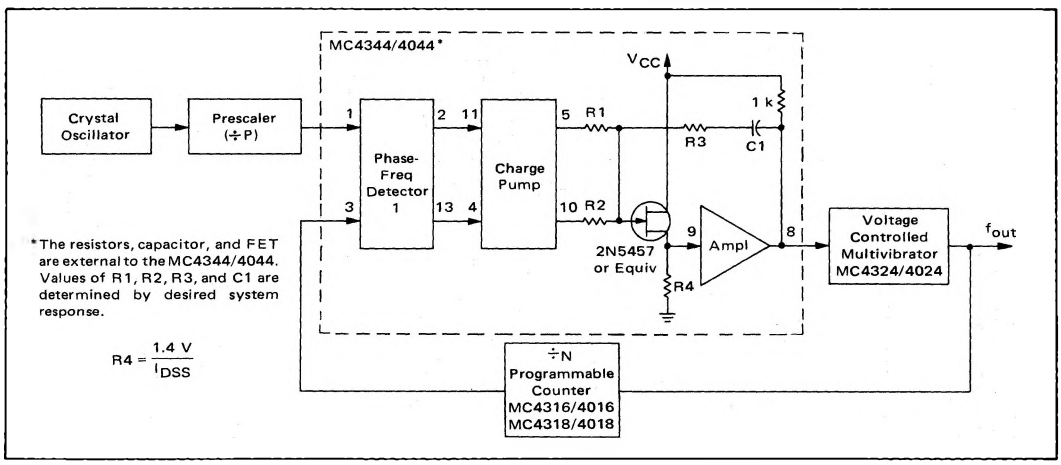


FIGURE 4 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP

Figure 4 shows the MC4316/4016 in a phase-locked loop with the MC4324/4024 and MC4344/4044. The loop has the following features:

1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phase-frequency detector 1 locks negative edges in the system;
2. Adjustable channel spacing, achieved by changing the pre-scaling factor (÷P) when generating the reference frequency;
3. Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.



INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4316/4318 INPUT LOADING FACTOR	MC4316/4318 OUTPUT LOADING FACTOR
MC4300	1.0	8.0
MC500	1.1	10
MC2100	0.75	6.6
MC3100	0.8	6.4
MC5400	1.0	8.0
MC9300	1.0	8.6
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 6 (2.0 k ohm pullup)	9.1

FAMILY	MC4016/4018 INPUT LOADING FACTOR	MC4016/4018 OUTPUT LOADING FACTOR
MC4000	1.0	8.0
MC400	1.0	8.0
MC2000	0.66	5.3
MC3000	0.8	6.4
MC7400	1.0	8.0
MC8300	1.0	8.6
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 6 (2.0 k ohm pullup)	8.3

*Due to logic "1" state drive limitations of the MDTL family.