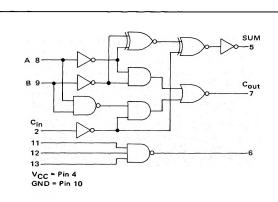
FULL ADDERS

MC4326F, L · MC4327F, L * MC4026F, L, P · MC4027F, L, P*



Input Loading Factor:

A, B = 2 C_{in}, Pins 11, 12, 13 = 1

Output Loading Factor: MC4326 = 15 MT

MC4326 = 15 MTTL | Loads MC4327 = 7 MTTL | Loads MC4026 = 12 MTTL | Loads

MC4027 = 6 MTTL | Loads

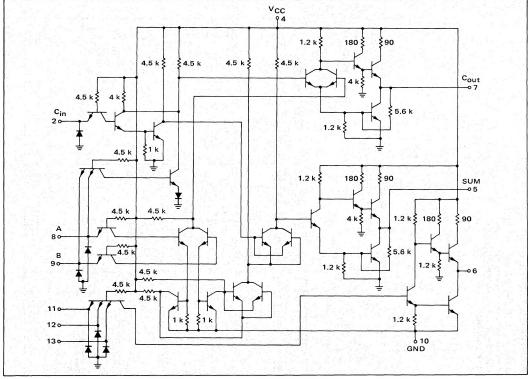
These full adders are designed for serial and ripple-carry parallel adder systems. True Sum and Carry are produced at the output from the input information. A separate 3-input NAND gate is provided on the monolithic chip to provide the inverted Sum or Carry output.

TRUTH TABLE

L _!	nput P	ins	Outpu	ıt Pins
8	9	2	5	7
Α	В	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Total Power Dissipation = 90 mW typ/pkg Add Delay = 25 ns typ Carry Delay = 13 ns typ

CIRCUIT SCHEMATIC



^{*}F suffix = TO-86 ceramic flat package (Case 607).

L suffix = TO-116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

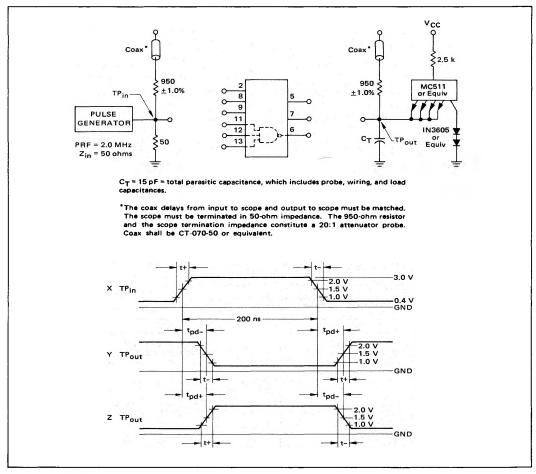
MC4326F,L, MC4327F,L, MC4026F,L,P, MC4027F,L,P (continued)

ELECTRICAL CHARACTERISTICS Test procedures are shown for inputs A and Cin. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.

																				•	5		2000					
6	4	7	5	7		ن	1										E	μA						Volts				
Š	7 [F	¢		7001							@ Test		_ [0]		-B		-	-					-	-	-
•		1	F	5)								Ę	Temperature	e Pr.	Std	Pr*	Std		ZI.	> "	ν Ε	٧*	V 1.	Vout	V	V _{CC}	
چ			1	_										(-55°C	20 C	10	-2.2	-1.2	,	٦	0.45 2	2.8 4.5	2.0	6.0	5.5	1	5.0	
12	7	8			-	, e					MC	MC4326", MC4327	AC4327	+25°C	C 20	10	-2.2	-1.2	1.0	2.0 0	0.45 2	2.8 4.5	1.7	7 1.0	5.5	8.0	5.0	
12			4				u							+125°C	C 20	10	-2.2	-1.2			0.45 2	2.8 4.5	1.4	4 0.8	5.5		5.0	
13		7	1	2			•							(00	20	10	-2.2	-1.2	,	,	0.45 3	3.0 4.5	9 1.9	9 1.0	5.5		5.0	
											WC	MC4026', MC4027	1C4027	+25°C	20 C	01	-2.2	-1.2	1.0	2.0	0.45 3	3.0 4.5	1.8	8 1.0	5.5	7.0	5.0	
										- 1				(+75°C		10	-2.2	-1.2	-	1	0.45 3	3.0 4.5	1.7	7 1.0	5.5	,	2.0	1 1
		ig		MC4326, MC4327 Test Limits	, MC43.	27 Test	Limits			MC40	26, MC	MC4026, MC4027 Test Limits	t Limits						TEST	URREN	T/VOLTA	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW	O PINS LIST	ED BELOW				
		Inder	−55°C	٥	+25°C	ړ	+125°C	٠	၀ွ		+25°C		+75°C						1	-	-		-	-			-	
Characteristic	Symbol	Test	Win	×	Min	×	Min	×	Min	×e	Min Max	×	, Max	Ę		loi.	_0	_8_	_5	2lin	ر ار	V _H	>	, V _{#0}	V _{oo} v	\ ×em ×	20	Gud
Input																												
Forward Current	ī.	2		-1.33	,	-1.33		-1.33	7	-1.66	7	-1.66	-I.66	6 mAdc	,.	,			1	,	,	- 8,9,11,12,13	- 12,13		_	•	4	2,10
		80	1	-2.66		-2.66		-2.66	7	-3.32	6,	-3.32	-3.32	2 mAdc		,			,	,	-	- 2,9,11,12,13		,			4	8,10
Leakage Current	I.	2		0.1	-	0.1	,	0.1	,	0.1	- 0	0.1	0.1	mAdc				,	-	,	-	- 2		•	,		4	8,9,10,11,12,13
		80	,	0.2	-	0.2	,	0.2	-	0.2	- 0	0.2	0.2	mAdc							,	8		,		-	4	2,9,10,11,12,13
Inverse Beta Current	I.	~		0.1		0.1	,	0.1	,	0.1	-	0.1	0.1	mAdc	0					,	,	- 2	-	'	,	,	4	10
		.00		0.2	,	0.2	,	0.2	, -	0.2	0	0.2	0.2	mAdc	,				,	,			-		,	'	4	10
Breakdown Voltage	BV	20			5.5		, '		,	- 2	5.5	-	1	Vdc		,			2			-	_	,	,	,	4	8,9,10,11,12,13
		7 00			_	Ö					_								27	1 0				. ,			4 4	2.9.10.11.12.13
		8			-	,	-					1	1	-				-	-	0 80							4	10
Output Output Voltage	Λ	တ		0.45	-	0.45	,	0.45	0	0.45	0	0.45	0.45	Vdc		. 4			- 1			,		9 8 9			4	OI.
	Vout "1"	2	2.5	,	2.4		2.5		2.5	2	2.4	2.5	- 9	Vdc				2	,		+		2	$^{\perp}$		'	4	10
Leakage Current	POLK	20		0.25	1	0.25	,	0.25	,	0.25	0.	0.25	0.25	mAdc						,	2,	2,8,9			2		4	10
Short-Circuit Current	JSC	2	-25	-100	-25	-100	-25	-100	-25 -	-100	-25 -1	-100 -25	-100	mAdc	to.	,			,		2,	2,8,9	'	<u>'</u>	-		4	5,10
Output Voltage	TO _A	S.		9.4		4.0	,	0.45	,	4.0	0	0.4	0.45	Vdc		25			,	,	2,8,9	,	'	'	•	,	4	10
	МОМ	10	2.8		3.1		3.15		3.0		3.1	3.15	2	Vdc				2	,	,	2,	2,8,9	-	1			4	10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4				38	, .			,	-	47 -	1	mAdc					,					-	1	4		2,8,9,10,11,12,13
Power Supply Drain	HGdI	4		2.2		2.7		2.7	,	35	-	35 -	35	mAdc					,				-	'	1	,	4	10
				-	-	-	-				-			-														

MC4326F,L, MC4327F,L, MC4026F,L,P, MC4027F,L,P (continued)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

	PINS			INPUT PIN				OUTPUT PIN			
TEST	UNDER TEST (In/Out)	8 A	9 B	11	12	13	5 SUM	6	7 C _{out}	ns max	
t _{pd+}	9/5	Open	×	Open	Open	Open	z	_	-	35	
tpd-	9/5	Open	×	Open	Open	Open	z	-	-	35	
t _{pd+}	11/6	Open	Open	×	3.0 V	3.0 V	- 1	Υ	-	20	
tpd-	11/6	Open	Open	×	3.0 V	3.0 ∨	- 1	Y	-	20	
t _{pd+}	8, 9/7	×	×	Open	Open	Open	- 1		Z	20	
tpd-	8, 9/7	×	×	Open	Open	Open	-		Z	20	
t+	1									8.0	
t-	7		Tested	during each of	the above tes	ts.				5.0	