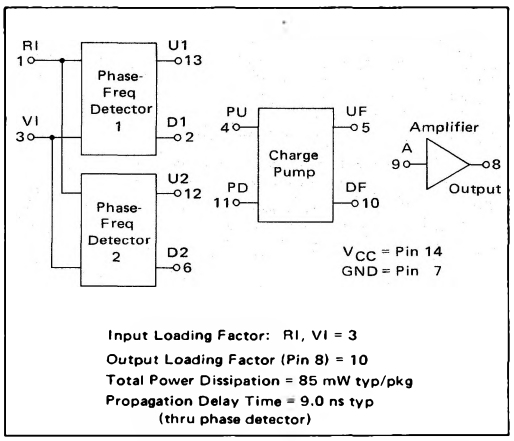
PHASE-FREQUENCY DETECTOR

MC4344F, L*
MC4044F, L, P*



Input Loading Factor: RI, VI = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked-loop applications.

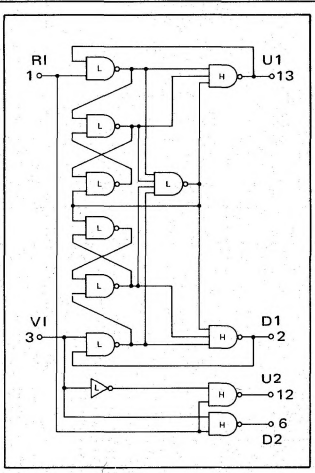
The two phase detectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

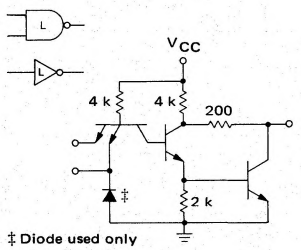
The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error.

PHASE DETECTOR

The phase detector portion of this device is constructed using low and high-level gates interconnected as shown by the logic diagram.

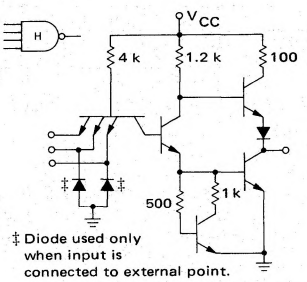


LOW-LEVEL "NAND" GATE



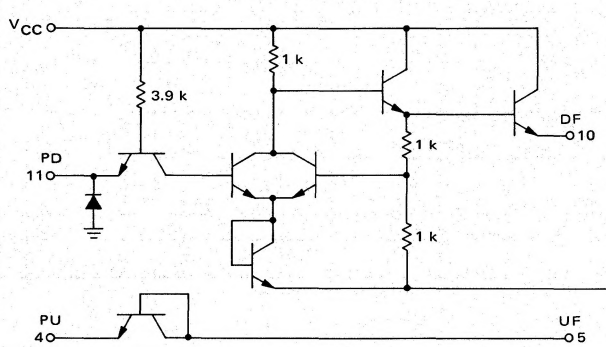
‡ Diode used only when input is connected to external point.

HIGH-LEVEL "NAND" GATE

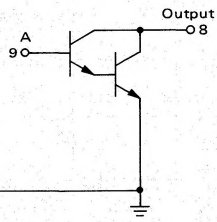


‡ Diode used only when input is connected to external point.

CHARGE PUMP



AMPLIFIER



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

MC4344F,L , MC4044F,L,P (continued)

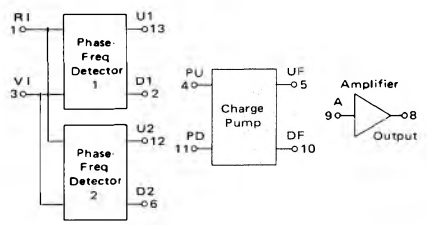
INPUT STATE	INPUT RI	INPUT VI	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

ELECTRICAL CHARACTERISTICS



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_D	I_A	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_D	I_A	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																																
Forward Current	I_F	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	14	–	7
		3	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	↓	–	–	–	–	–	–	–	–	3	–	–	–	–	↓	–	↓
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	–	11	–	–	–	–		–	
Leakage Current	I_R	1	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	1	–	–	–	14	–	7
		3	–	120	–	120	–	120	–	120	–	120	–	120		–	–	–	–	–	–	–	–	–	3	–	–	–	14	–	7
		4	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0		–	–	–	–	–	–	–	–	–	–	–	–	–	4	–	5,7
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	–	11	–	–	–	14	–	7
Breakdown Voltage	BV_{in}	1	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	↓	–	–	–	–	–	↓	–	–	–	↓	–	–	–	3	–	–	–	–	–	–	–	–	–	↓	–	↓
		11	–	–		–	–	–	–	–		–	–	–		–	–	–	11	–	–	–	–	–	–	–	–	–		–	
Clamp Voltage	V_D	1	–	–	-1.5	–	–	–	–	–	-1.5	–	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	-1.5	–	–	–	–	–	-1.5	–	–	–	Vdc	–	–	–	–	3	–	–	–	–	–	–	–	–	14	–	7
Output (Note 1)																																
Output Voltage	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	–	–	1.3	–	–	–	–	–	14	–	–	7
	V_{OH}	12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	1.3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	12	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	12	–	–	–	–	–	–	1	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	1.3	–	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
Short-Circuit Current	I_{SC}	2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	3	1	–	–	–	–	–	–	–	14	2,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		–	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	–	6,7
		12														–	–	–	–	–	–	1,3	–	–	–	–	–	–	–	–	–	7,12
		13														–	–	–	–	–	–	3	1	–	–	–	–	–	–	–	–	7,13
Leakage Current	I_{OLK}	2	–	250	–	250	–	250	–	250	–	250	–	250	μAdc	–	–	–	–	–	–	3	1	–	–	–	–	14	–	–	–	7
		6	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	1,3	–	–	–	–	–	↓	–	–	–	↓
		12	–		–		–		–		–		–			–	–	–	–	–	–	1,3	–	–	–	–	–		–	–	–	
		13	–		–		–		–		–		–			–	–	–	–	–	–	3	1	–	–	–	–		–	–	–	
Collector-Emitter Voltage	V_{CE}	5	–	–	0.5	–	–	–	–	–	0.5	–	–	–	Vdc	–	–	–	5	–	–	–	–	–	–	–	–	–	–	–	–	4,7
Output Voltage	V_{EH}	10	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	Vdc	–	–	10	–	–	–	11	–	–	–	–	–	14	–	–	7
Output Current	I_O	8	0.2	–	0.8	–	1.0	–	0.5	–	0.8	–	1.0	–	mAdc	–	–	–	–	–	9	–	–	–	–	–	–	–	8	–	7
Leakage Current	I_{OLK}	8	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	–	–	–	–	8	–	7,9
		10	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	μAdc	–	–	–	–	–	–	–	–	–	11	10	–	–	14	–	7
Power Requirements (Total Device)																																
Power Supply Drain	I_{PD}	14	–	40	–	40	–	40	–	40	–	40	–	40	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	14	–	–	7	

Note 1. The outputs of the device must be tested by sequencing through the indicated input states according to the truth table and functional diagram. All input, power supply and ground voltages must be maintained between tests unless otherwise noted. Procedures identified by a double asterisk (**) in the Symbol column are necessary to change the state of the sequential logic.

Pulse 1: V_{CCL} ⌐ V_{CC} Used to change power supply voltage from previous test.

APPLICATIONS INFORMATION

FIGURE 1 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP

Figure 1 shows the MC4344/4044 in a phase-locked loop with the following features:

1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phase-frequency detector 1 locks negative edges in the system;
2. Adjustable channel spacing, achieved by changing the prescaling factor (÷ P) when generating the reference frequency;
3. Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.

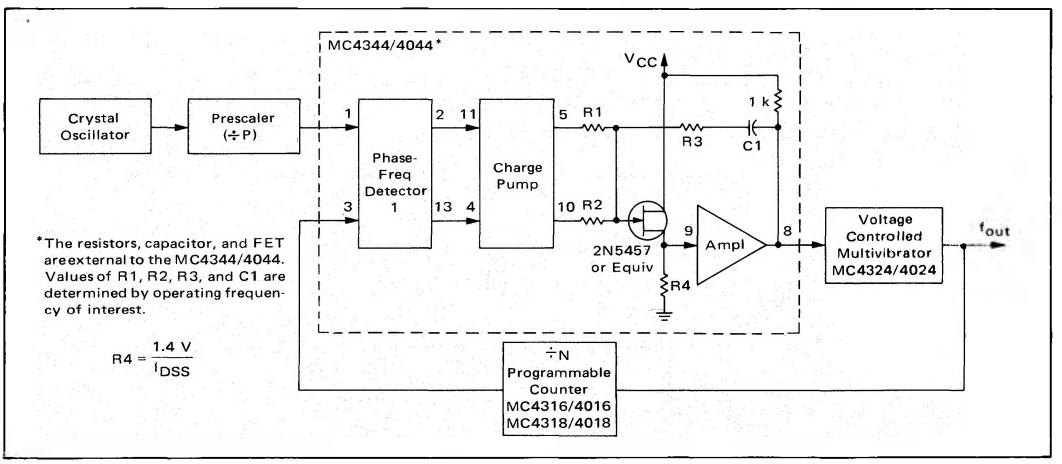
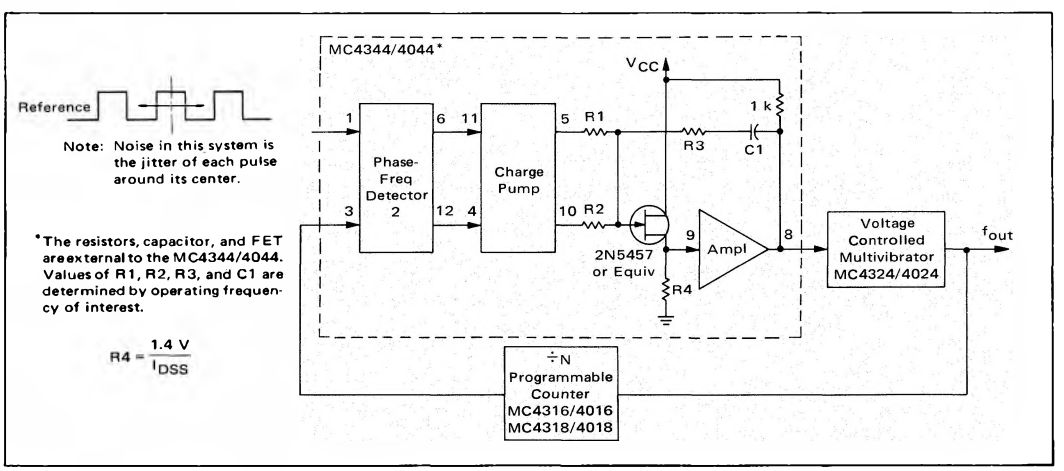


Figure 2 shows phase detector 2 of the MC4344/4044, which operates as a correlation detector, used in a phase-locked loop. There are two differences between this system and that shown in Figure 1. First, the VCM output, when locked in, lags the reference by 90°. Second, since the correlation detector integrates the product of its two inputs over each cycle, it can handle signals in a high-noise environment. This loop is sensitive to harmonics, therefore care must be taken to limit the frequency range of the VCM.

FIGURE 2 – PHASE-LOCKED, CORRELATION DETECTOR LOOP



APPLICATIONS INFORMATION (continued)

FIGURE 3 – SLAVE CLOCK PULSE GENERATOR

Figure 3 depicts the MC4344/4044 in a system used to generate a slave clock pulse with its negative edge locked to the negative edge of the master clock, but with adjustable pulse width. The pulse width of the slave clock pulse is controlled only by the monostable multivibrator, which is triggered from the negative edge of an input pulse.

The slave clock application is useful when the clock from a master computer must be slaved to that of a satellite.