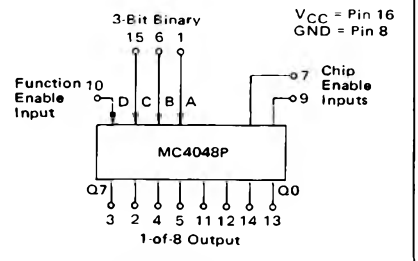
NON-INVERTING
ONE-OF-EIGHT DECODER

MC4048P*



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Total Power Dissipation
= 240 mW typ/pkg

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

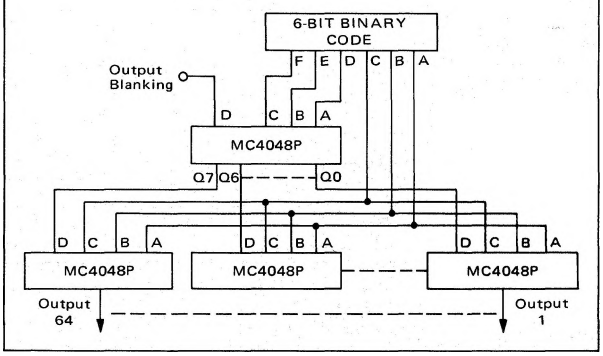
E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							

The MC4048P is derived from the XC171 128-bit Read Only Memory. A 3-bit binary address selects the desired word for the 8-bit output, and the selected output goes to a logic "1". The function enable input, D, is useful for expansion of the decoding function. When D is a logic "0" all outputs are logic "0". A logic "1" on D produces a logic "1" on the selected output.

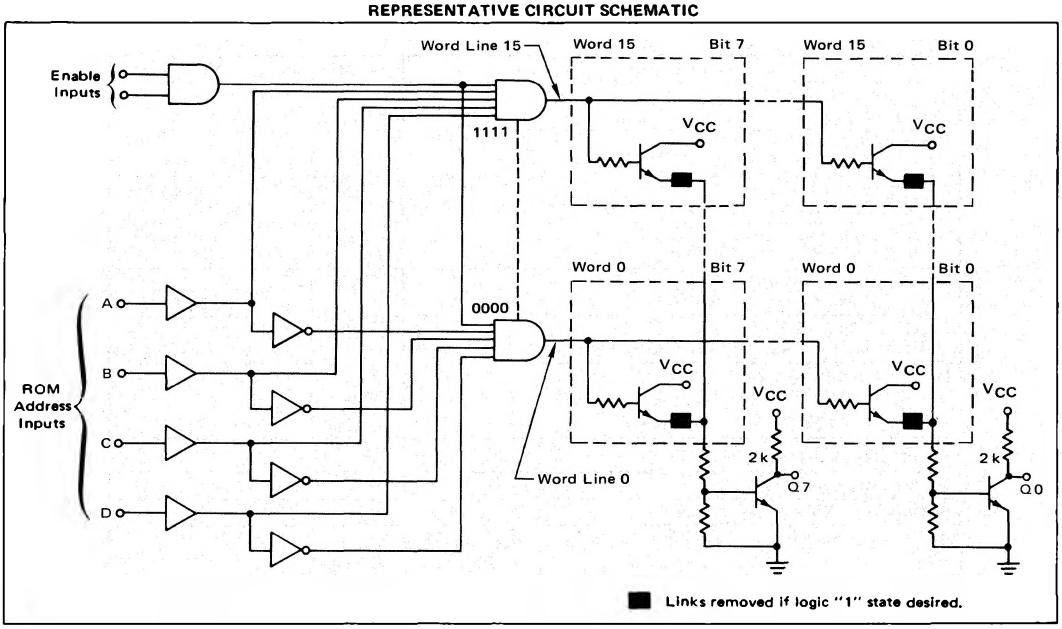
Features:

- Address times < 50 ns
- Outputs sink 16 mA
- Output capacitance < 7.0 pF @ 1.5 V

1-OF-64 DECODER
(Selected output is a positive logic "1")



REPRESENTATIVE CIRCUIT SCHEMATIC



*P suffix = 16-pin dual in-line plastic package (Case 612).

MC4048P (continued)

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4048 INPUT LOADING FACTOR	MC4048 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	7
MC3000	0.7	7
MC7400	1.0	10
MC830	1.15**	11

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 16 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Voltage (I_{OH} = 0.5 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OH}	2.5	-	Vdc
Power Supply Drain Current (Memory Enabled, V_{CC} = 5.25 Vdc)	$I_{PD\ max}$	-	85	mAdc
(Memory Disabled, V_{CC} = 5.25 Vdc)	$I_{PD\ min}$	-	55	

SWITCHING TIMES (V_{CC} = 5.0 Vdc)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t_{A+B+}	-	50	ns
Negative Input Address to Negative Output		t_{A-B-}	-	50	ns
Positive Input Address or Enable to Negative Output		t_{A+B-} or t_{E+B-}	-	50	ns
Negative Input Address or Enable to Positive Output		t_{A-B+} or t_{E-B+}	-	50	ns