

## MC4051 ${ }^{*}$

## Advance Information

This device is a monolithic MSI integrated circuit combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. The counter advances on the negative edge of the Clock, subject to control by the $\overline{\text { Enable input. The Serial Output is high driving the ninth }}$ count, allowing synchronous or asynchronous counter operation when used in conjunction with the Enable input and some external gating. The counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. This feature gives automatic suppression of leading zeros in the display. The latch section admits information while the Strobe is high and latches the data on the neg-
ative edge of the strobe. The seven-segment decoder/ driver is active high and will source up to 40 mA at a $10 \%$ duty cycle or 15 mA at a $100 \%$ duty cycle. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available.

The output structure of this device is an open emitterfollower configuration whose equivalent circuit is a voltage source with a relatively small series resistance. Although this resistance increases when the output is grounded, the situation is potentially destructive to the device. When the outputs are in the high (" 1 ") state, they should not be connected to ground through an impedance of less than 100 ohms.


[^0]
[^0]:    P suffix = 16-pin dual in-line plastic package (Case 612).
    This is advance information on a new introduction and specifications are subject to change without notice.

