

16-BIT SCRATCH PAD MEMORY CELL

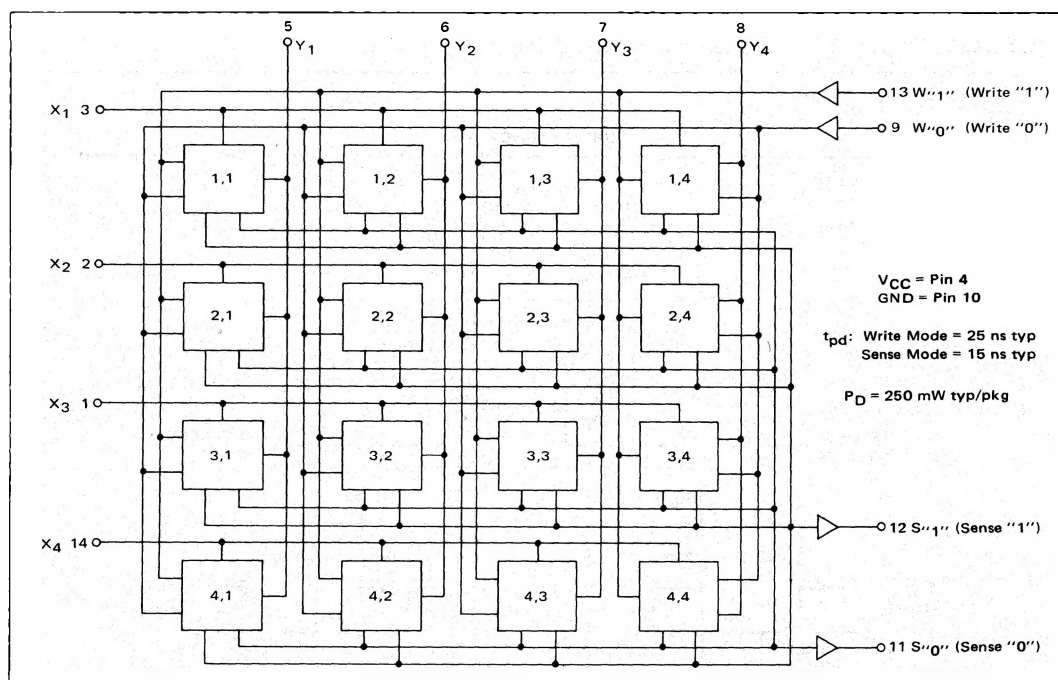
MEMORIES

MC4304F,L • MC4305F,L* MC4004F,L,P • MC4005F,L,P*

This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

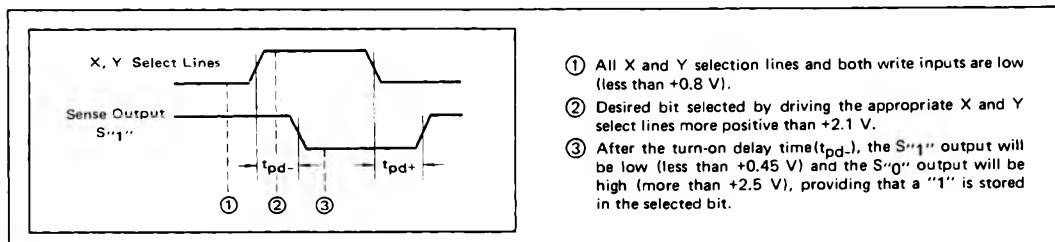
The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by

driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



— OPERATING SEQUENCE —

FIGURE 1 — READ MODE TIMING DIAGRAM

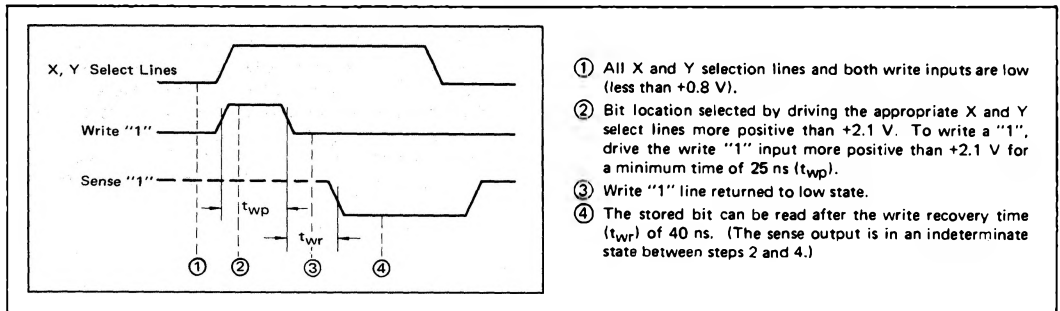


*F suffix = TO-86 ceramic flat package (Case 607).

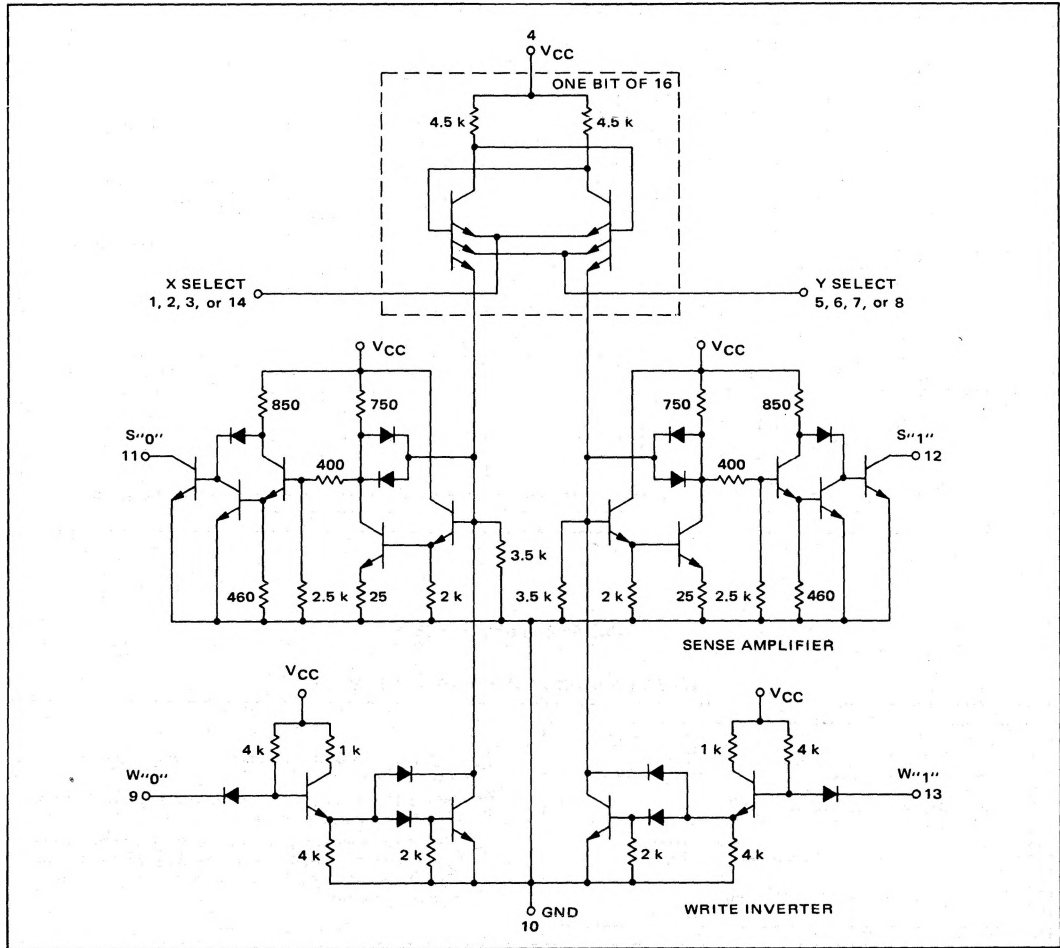
L suffix = TO-116 ceramic dual in-line package (Case 632).

P suffix = TO-116 plastic dual in-line package (Case 605).

FIGURE 2 - WRITE MODE TIMING DIAGRAM



CIRCUIT SCHEMATIC



MC4304F,L, MC4305F,L /MC4004F,L,P, MC4005F,L,P (continued)

ELECTRICAL CHARACTERISTICS

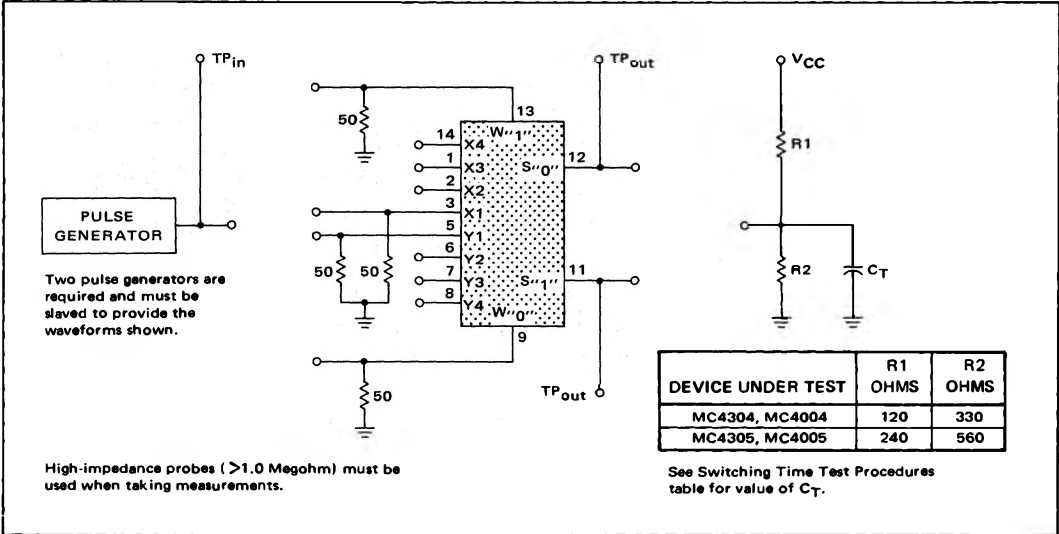
Test procedures are shown for only one bit. Other bits are tested in the same manner.

[illegible]

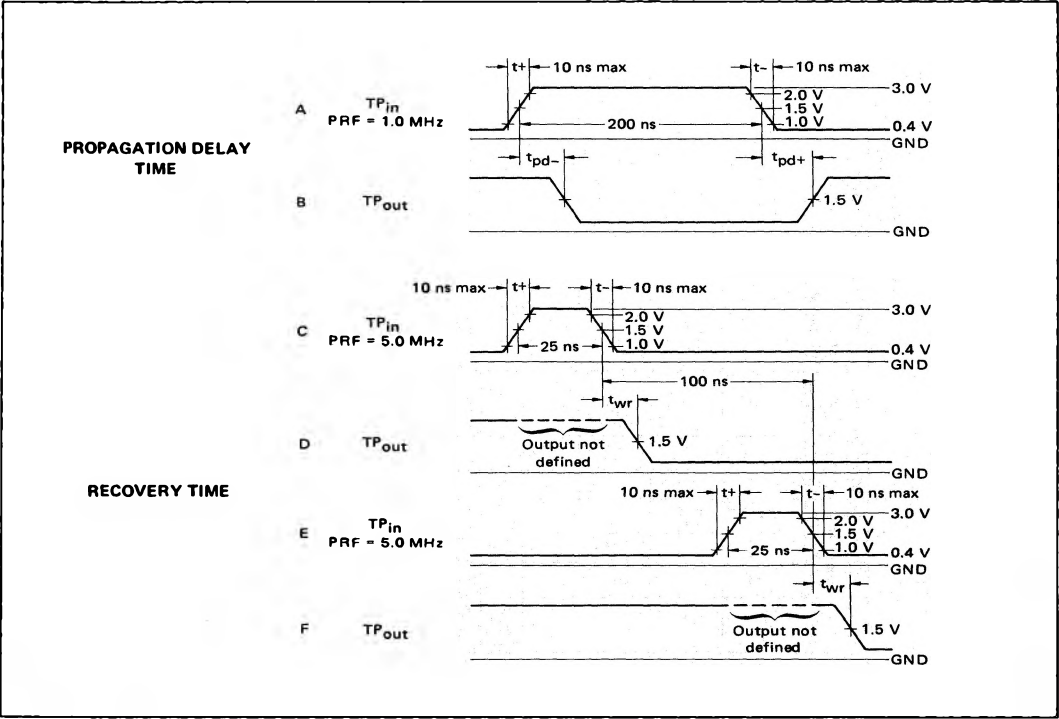
*Prime Fan-Out
Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. Procedures identified by a double asterisk (**) are preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

MC4304F,L, MC4305F,L /MC4004F,L,P, MC4005F,L,P (continued)

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



MC4304F,L, MC4305F,L /MC4004F,L,P, MC4005F,L,P (continued)

SWITCHING TIME TEST PROCEDURES (Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		Limits		
			3 X ₁	2 X ₂	1 X ₃	14 X ₄	5 Y ₁	6 Y ₂	7 Y ₃	8 Y ₄	9 W ₀	13 W ₁	11 S ₀	12 S ₁	C _T [*] pF	MC4304-5 ns max	MC4004-5 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	—	—	—	—	—
	t _{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	—	30	23	23
	t _{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	—	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	—	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	—	—	—	—	—
	t _{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	30	23	23	23
	t _{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	200	35	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	—	—	—	—	—
	t _{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	—	30	23	23
	t _{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	—	200	35	35
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	—	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	—	—	—	—	—
	t _{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	30	23	23	23
	t _{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	200	35	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	—	—	—	—	—
	t _{pd+}	11	A	Gnd	Gnd	Gnd	A	A	A	A	A	Gnd	Gnd	B	—	30	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	—	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	—	—	—	—	—
	**	—	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	—	—	—	—
	t _{pd+}	12	A	Gnd	Gnd	Gnd	A	A	A	A	A	Gnd	Gnd	B	30	35	35
Write Recovery Time	t _{wr}	12	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	—	D	30	40	40
		11	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	—	30	40	40
Write Pulse Width	t _{wp}	—	Tested during t _{wr} tests.													ns min	ns min
																25	25

*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.