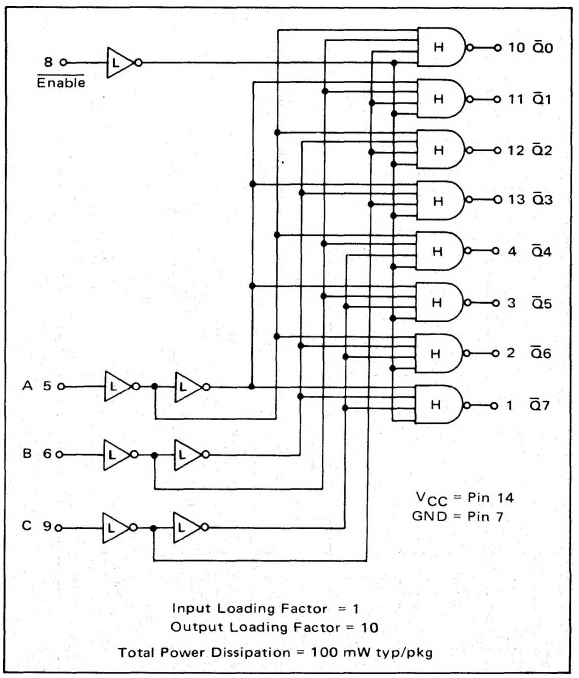
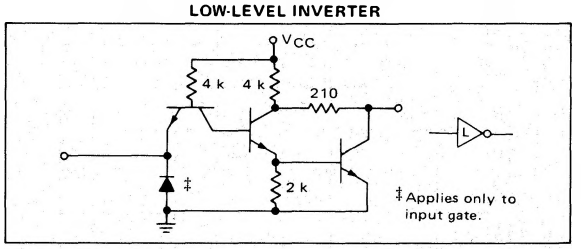
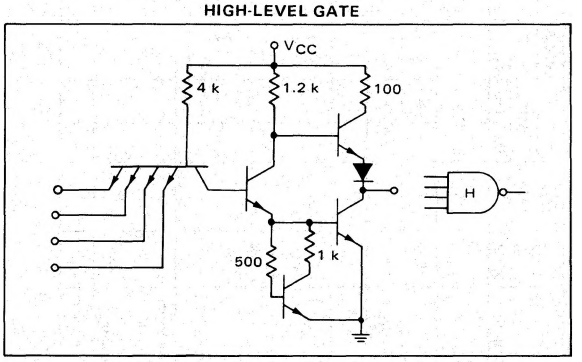
MC4306F,L*
MC4006F,L,P*



LOW-LEVEL INVERTER



HIGH-LEVEL GATE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 dual in-line ceramic package (Case 632).
P suffix = TO-116 dual in-line plastic package (Case 605).

This device converts three lines of input data to a one-of-eight output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The 3-input/8-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

$\bar{E}$ = 0

TRUTH TABLE

C	B	A	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

1 = High State
0 = Low State

TYPICAL TURN-ON DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

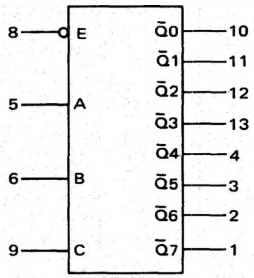
INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	11.5	16.0	11.5	16.0	11.5	16.0	11.5	16.0
B	11.5	11.5	16.0	16.0	11.5	11.5	16.0	16.0
C	11.5	11.5	11.5	11.5	16.0	16.0	16.0	16.0
$\bar{E}$	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	14.0	19.5	14.0	19.5	14.0	19.5	14.0	19.5
B	14.0	14.0	19.5	19.5	14.0	14.0	19.5	19.5
C	14.0	14.0	14.0	14.0	19.5	19.5	19.5	19.5
$\bar{E}$	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner. Additionally, test all input-output combinations according to the truth table.



@Test Temperature		I_{OL1} mA	I_{OL2} mA	I_{OH} mA	I_{in} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{RH} Volts	V_{max} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts
MC4306	−55°C	18.4	16	-1.6	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
	+25°C	18.4	16	-1.6	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
	+125°C	18.4	16	-1.6	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC4006	0°C	17.6	16	-1.6	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25
	+25°C	17.6	16	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25
	+75°C	17.6	16	-1.6	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4306 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4006 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_F	5	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	7
Leakage Current	I_R	5	-	40	-	40	-	40	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	7
Breakdown Voltage	BV_{in}	5	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	5	-	-	-	-	-	-	-	-	-	14	7
Clamp Voltage	V_D	5	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	5	-	-	-	-	-	-	-	14	-	7
Output																													
Output Voltage	V_{OL1}	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	1	-	-	-	-	8	5,6,9	-	-	-	-	-	-	14	7
	V_{OL2}	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	-	1	-	-	-	8	5,6,9	-	-	-	-	-	14	-	7
	V_{OH}	1	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	1	-	-	-	5,6,8,9	-	-	-	-	-	14	-	7
Short-Circuit Current	I_{SC}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	8	-	14	-	-	1,7
Power Requirements (Total Device)																													
Maximum Power Supply Current	I_{max}	14	-	-	-	51	-	-	-	-	-	51	-	-	mAdc	-	-	-	-	-	-	-	-	-	5,6,8,9	14	-	-	-	7
Power Supply Drain	I_{PD}	14	-	-	-	34	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	8	-	5,6,9	-	14	-	-	7

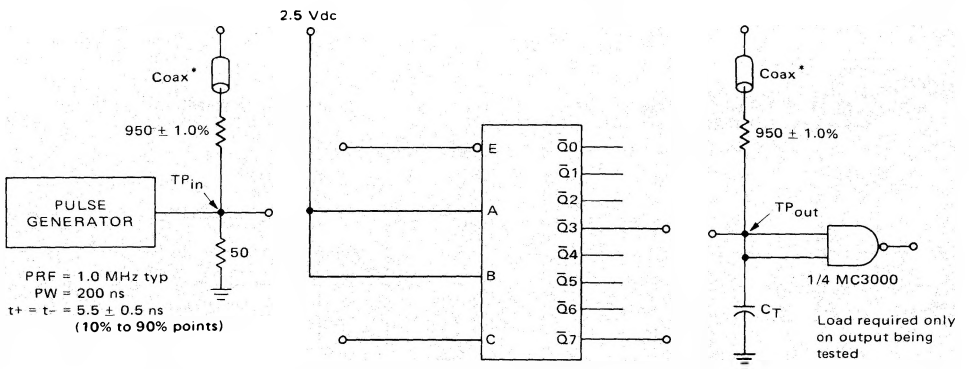
INPUT AND OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4306 INPUT LOADING FACTOR	MC4306 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.2	12
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4006 INPUT LOADING FACTOR	MC4006 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.8	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

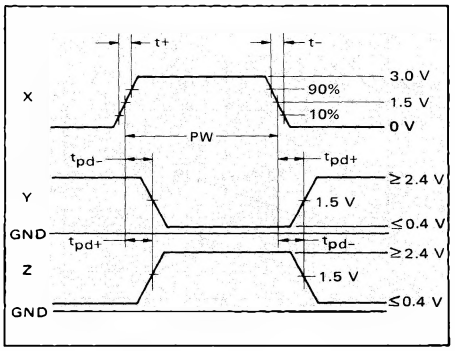
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	Ē	C	Q̄3	Q̄7	LIMITS Max	LIMITS Unit
t_{pd+} (C to Q̄3)	Gnd	X	Z	–	20	ns
t_{pd-} (C to Q̄3)	Gnd	X	Z	–	17	ns
t_{pd+} (C to Q̄7)	Gnd	X	–	Y	29	ns
t_{pd-} (C to Q̄7)	Gnd	X	–	Y	23	ns
t_{pd+} (Ē to Q̄7)	X	2.5 V	–	Z	21	ns
t_{pd-} (Ē to Q̄7)	X	2.5 V	–	Z	20	ns

VOLTAGE WAVEFORMS



TYPICAL SWITCHING TIMES

FIGURE 1 – TURN-ON DELAY TIME versus TEMPERATURE

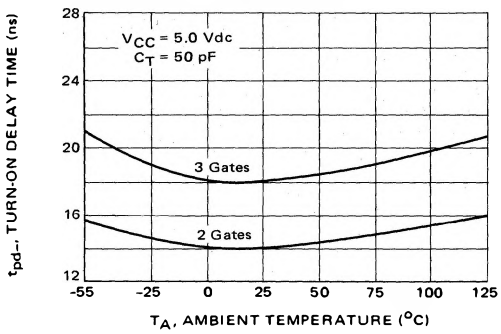


FIGURE 2 – TURN-OFF DELAY TIME versus TEMPERATURE

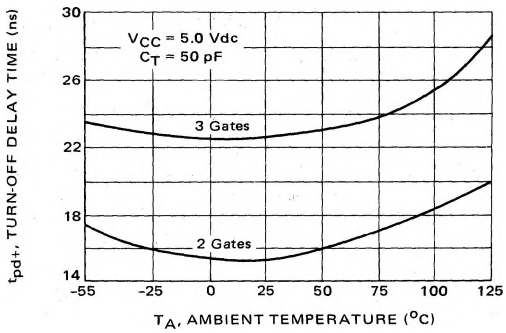


FIGURE 3 – TURN-ON DELAY TIME versus TEMPERATURE

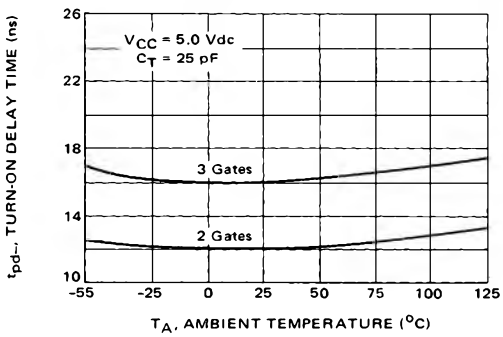


FIGURE 4 – TURN-OFF DELAY TIME versus TEMPERATURE

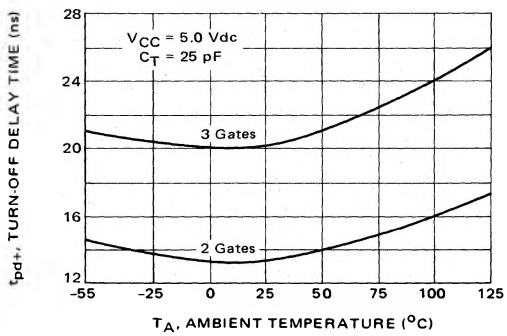


FIGURE 5 – TURN-ON DELAY TIME versus CAPACITIVE LOADING

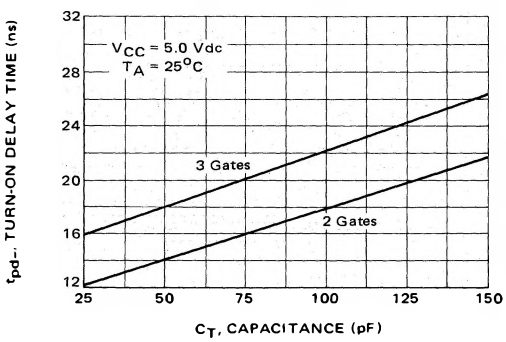
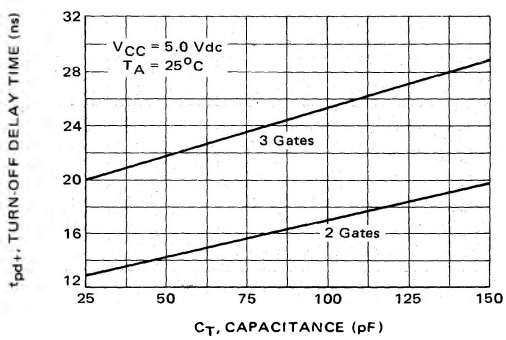


FIGURE 6 – TURN-OFF DELAY TIME versus CAPACITIVE LOADING



TYPICAL SWITCHING TIMES (continued)

FIGURE 7 – TURN-ON DELAY TIME versus POWER SUPPLY VOLTAGE

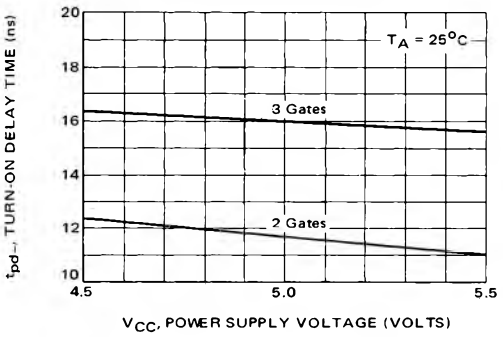
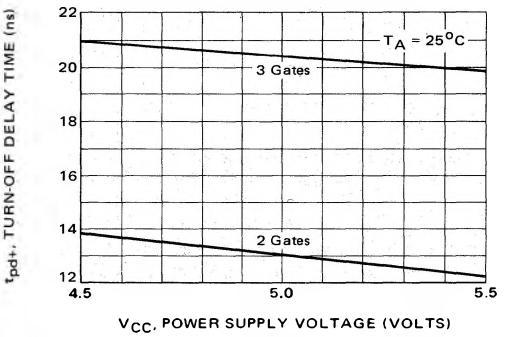


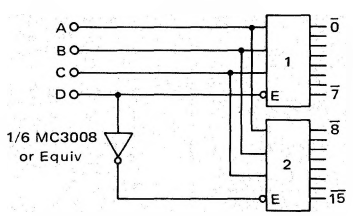
FIGURE 8 – TURN-OFF DELAY TIME versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

Combinations of MC4306/4006 decoders can be used to produce various decoding operations. Figure 1 illustrates the use of two of these binary to one-of-eight decoders and one inverter to convert four digital inputs into one of 16 mutally exclusive outputs. In this operation the $\overline{\text{Enable}}$ input of both decoders, in conjunction with the inverter, is used for the fourth digital bit. The D input is low from state 0 thru 7, enabling decoder unit 1 and inhibiting decoder unit 2. For states 8 thru 15 the reverse is true, thus providing the eight additional states needed for the fourth input variable. Outputs $\overline{0}$ thru $\overline{15}$ are selected by the natural binary code on inputs A, B, C, and D; however, the MC4306/4006 can be used to decode any four-bit code by appropriately choosing outputs to correspond to the inputs.

FIGURE 1 – BINARY TO 1-OF-16 DECODER



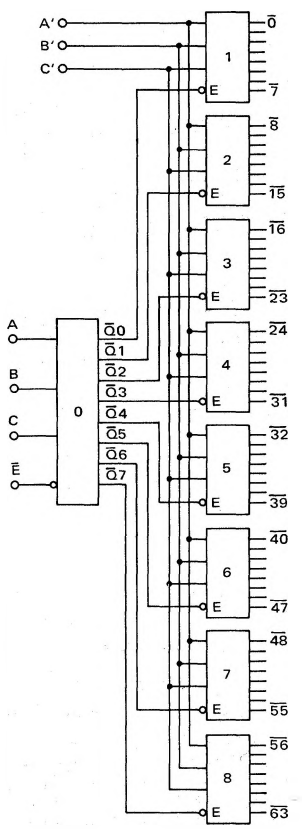
Output Terminal	Input D	C	B	A	Output Device
0	0	0	0	0	1
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	2
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

TYPICAL APPLICATIONS
(continued)

Figure 2 illustrates the use of nine MC4306/4006 decoders in a 1-of-64 decoder.

If the $\overline{\text{Enable}}$ input is used as a data input terminal, the data bit will appear at the output terminal selected by the address on lines A, B, and C. Thus the MC4306/4006 can be used as an eight-line data distributor (demultiplexer). All unselected outputs will be at a logic "1" level. Figure 3 shows two MC4312/4012 four-bit shift registers used in conjunction with an MC4306/4006 to yield an eight-bit serial data transmission system. The MC4312/4012's convert eight bits of parallel data to serial for transmission to another part of the system. The MC4306/4006 receives the serial data and distributes it to any of eight locations. By holding the address lines of the MC4306/4006 constant, all data bits are routed to the same location where they may be converted to parallel form again. By changing the MC4306/4006 address inputs at the same rate that data is being transmitted, each data bit can be distributed to a different location.

FIGURE 2 – GATED BINARY TO 1-OF-64 DECODER



Output Terminal	Input C	B	A	C'	B'	A'	Output Device
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	
2	0	0	0	0	1	0	
3	0	0	0	0	1	1	
4	0	0	0	1	0	0	
5	0	0	0	1	0	1	
6	0	0	0	1	1	0	
7	0	0	0	1	1	1	
8	0	0	1	0	0	0	2
9	0	0	1	0	0	1	
10	0	0	1	0	1	0	
11	0	0	1	0	1	1	
12	0	0	1	1	0	0	
13	0	0	1	1	0	1	
14	0	0	1	1	1	0	
15	0	0	1	1	1	1	
16	0	1	0	0	0	0	3
17	0	1	0	0	0	1	
18	0	1	0	0	1	0	
19	0	1	0	0	1	1	
20	0	1	0	1	0	0	
21	0	1	0	1	0	1	
22	0	1	0	1	1	0	
23	0	1	0	1	1	1	
24	0	1	1	0	0	0	4
25	0	1	1	0	0	1	
26	0	1	1	0	1	0	
27	0	1	1	0	1	1	
28	0	1	1	1	0	0	
29	0	1	1	1	0	1	
30	0	1	1	1	1	0	
31	0	1	1	1	1	1	
32	1	0	0	0	0	0	5
33	1	0	0	0	0	1	
34	1	0	0	0	1	0	
35	1	0	0	0	1	1	
36	1	0	0	1	0	0	
37	1	0	0	1	0	1	
38	1	0	0	1	1	0	
39	1	0	0	1	1	1	
40	1	0	1	0	0	0	6
41	1	0	1	0	0	1	
42	1	0	1	0	1	0	
43	1	0	1	0	1	1	
44	1	0	1	1	0	0	
45	1	0	1	1	0	1	
46	1	0	1	1	1	0	
47	1	0	1	1	1	1	
48	1	1	0	0	0	0	7
49	1	1	0	0	0	1	
50	1	1	0	0	1	0	
51	1	1	0	0	1	1	
52	1	1	0	1	0	0	
53	1	1	0	1	0	1	
54	1	1	0	1	1	0	
55	1	1	0	1	1	1	
56	1	1	1	0	0	0	8
57	1	1	1	0	0	1	
58	1	1	1	0	1	0	
59	1	1	1	0	1	1	
60	1	1	1	1	0	0	
61	1	1	1	1	0	1	
62	1	1	1	1	1	0	
63	1	1	1	1	1	1	

FIGURE 3 – 8-LINE MULTIPLEXED TRANSMISSION SYSTEM

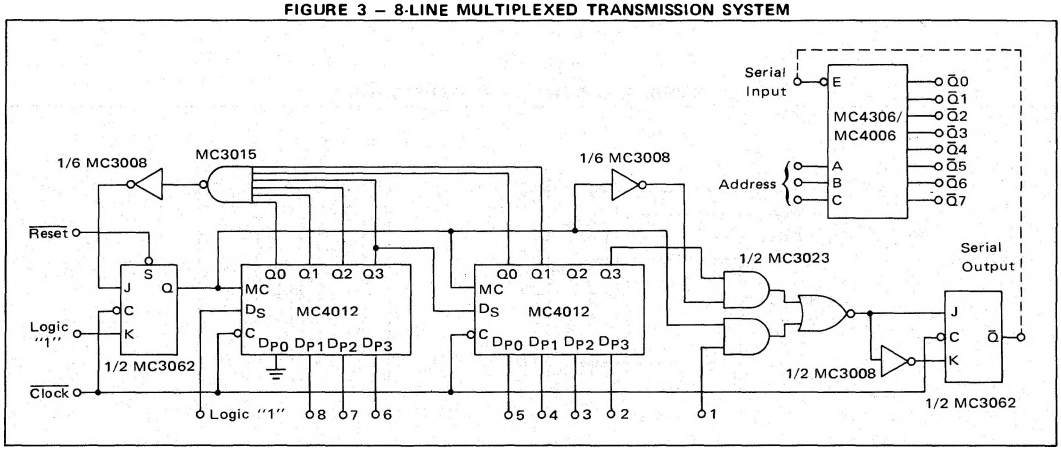
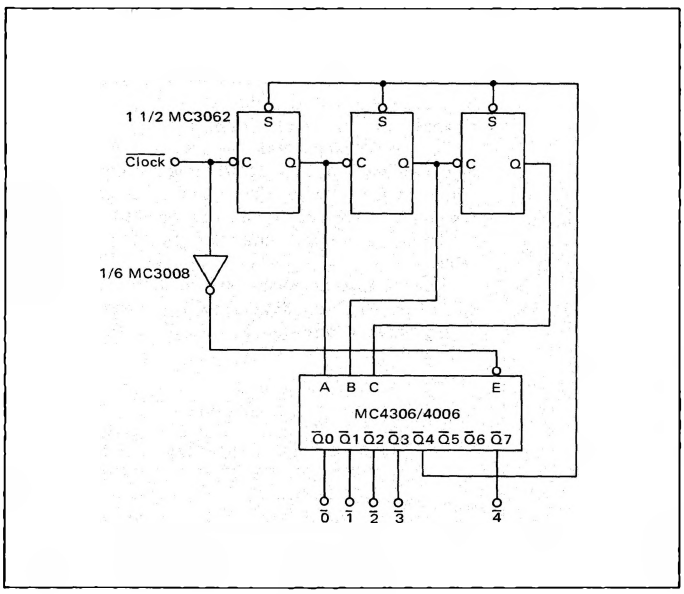


FIGURE 4 – DECODED DIVIDE-BY-FIVE COUNTER



TYPICAL APPLICATIONS
(continued)

In addition to simply decoding the output state of a counter, the MC4306/4006 can be used to make an ordinary binary counter into an odd-modulus counter. For example, three flip-flops and one MC4306/4006 provide a completely decoded divide-by-five counter as shown in Figure 4. The $\overline{4}$ output is used to set all the flip-flops to the 111 state so that the counter will return to 000 on the next clocking edge. The $\overline{\text{Enable}}$ input is used to prevent false outputs due to rippling of the outputs through intermediate states. Output 7 of the MC4306/4006 is used for the fifth counter output state.