MC4328F,L thru MC4331F,L*
MC4028F,L,P thru MC4031F,L,P*

CONDENSED TRUTH TABLE FOR THE Nth STAGE

Pin Numbers 8	9	11	12,13	13, 14, 1	5	6	7		
A_n	B_n	$C_{in1(n-1)}$	Note 1	Note 2	Sum	$\oplus_{out}$	MC4330/4030 MC4331/4031 C_{out}	MC4328/4028 MC4329/4029 C_{out}	Comment Note 3
0	0	0	0	0	0	0	0	0	–
0	0	0	0	1	1	0	0	0	–
0	0	0	1	0	1	0	0	0	–
0	0	0	1	1	1	0	0	0	ϕ
0	0	1	0	0	1	0	0	0	–
0	0	1	0	1	1	0	0	0	–
0	0	1	1	0	1	0	0	0	ϕ
0	0	1	1	1	1	0	0	0	ϕ
0	1	0	0	0	1	1	0	0	–
0	1	0	0	1	0	1	0	1	–
0	1	0	1	0	0	1	0	1	–
0	1	0	1	1	0	1	0	1	ϕ
0	1	1	0	0	0	1	0	1	–
0	1	1	0	1	0	1	0	1	ϕ
0	1	1	1	0	0	1	0	1	ϕ
0	1	1	1	1	0	1	0	1	ϕ
1	0	0	0	0	1	1	0	0	–
1	0	0	0	1	0	1	0	1	–
1	0	0	1	0	0	1	0	1	–
1	0	0	1	1	0	1	0	1	ϕ
1	0	1	0	0	0	1	0	1	–
1	0	1	0	1	0	1	0	1	ϕ
1	0	1	1	0	0	1	0	1	ϕ
1	0	1	1	1	0	1	0	1	ϕ
1	1	0	0	0	0	0	1	1	–
1	1	0	0	1	1	0	1	1	–
1	1	0	1	0	1	0	1	1	–
1	1	0	1	1	1	0	1	1	ϕ
1	1	1	0	0	1	0	1	1	–
1	1	1	0	1	1	0	1	1	ϕ
1	1	1	1	0	1	0	1	1	ϕ
1	1	1	1	1	1	0	1	1	ϕ

Note 1. This column represents the AND function whose inputs are pins 13 and 12, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(C_{in\,(n-2)})$.

Note 2. This column represents the AND function whose inputs are pins 13, 14, and 1, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(A_{n-2} \oplus B_{n-2})(C_{n-3})$.

Note 3. ϕ = Don't Care. The "Don't Care" occurs for the MC4330-31/4030-31 only, because the C_n and the $\oplus_n$ from any one previous stage entering a given subsequent stage cannot be simultaneously at logic "1".

This family of fast adders is designed for use in parallel look-ahead carry adder applications where high-speed addition is required. The dependent-carry fast adders have a Carry output that is dependent upon the two input bits for that stage plus the Carry input from all previous stages. The Carry output from the MC4330/31 is independent of the carry from the previous stages.

Input Loading Factor:
$\oplus_{in1}$, A, B = 2
$\oplus_{in2}$, C_{in1}, C_{in2}, C_{in3} = 1

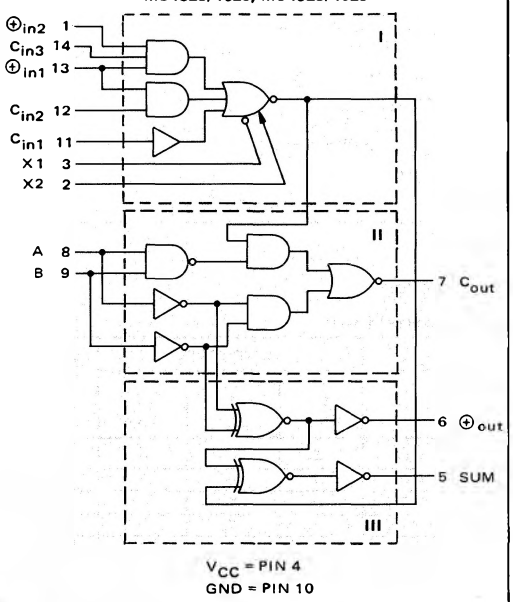
Output Loading Factor:
MC4328, MC4330 = 15 MTTL I Loads
MC4329, MC4331 = 7 MTTL I Loads
MC4028, MC4030 = 12 MTTL I Loads
MC4029, MC4031 = 6 MTTL I Loads

Total Power Dissipation = 125 mW typ/pkg

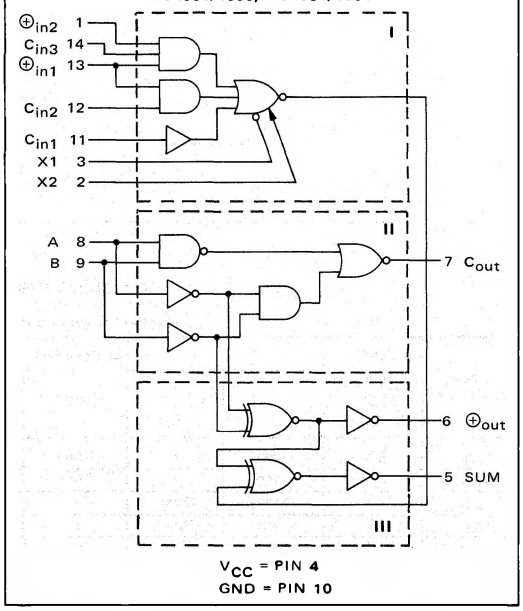
Add Delay = 25 ns typ

Carry Delay = 13 ns typ

DEPENDENT-CARRY FAST ADDER
MC4328/4028, MC4329/4029

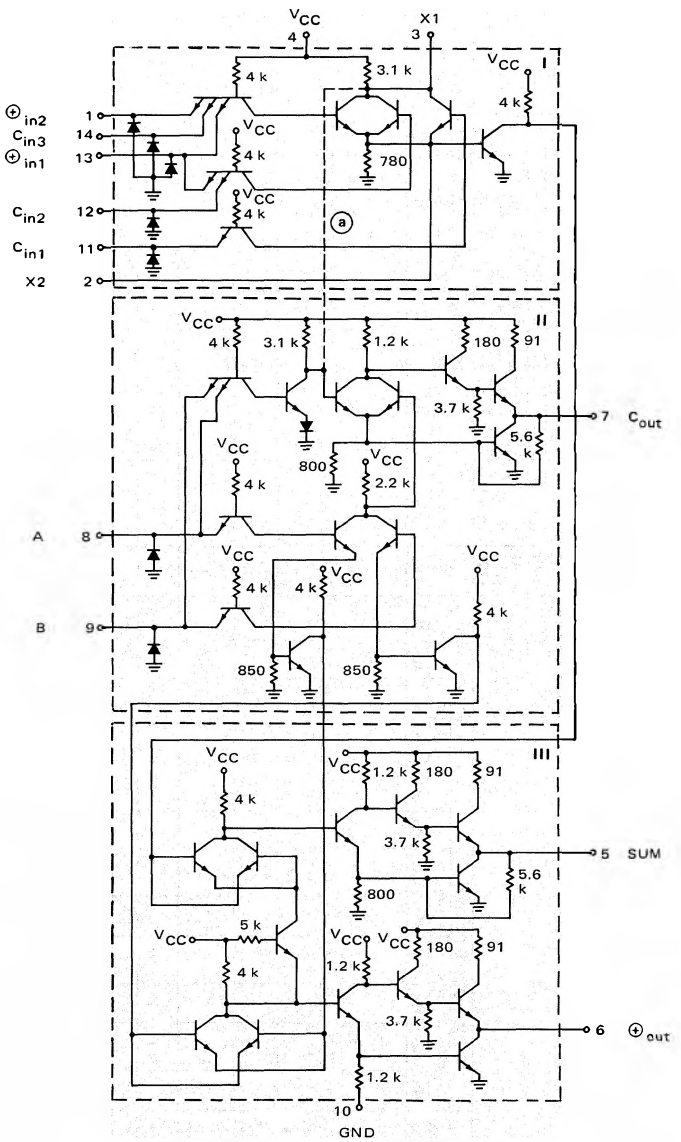


INDEPENDENT-CARRY FAST ADDER
MC4330/4030, MC4331/4031



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

CIRCUIT SCHEMATIC



(a) Connection shown by dashed line used only on dependent-carry devices.

ELECTRICAL CHARACTERISTICS

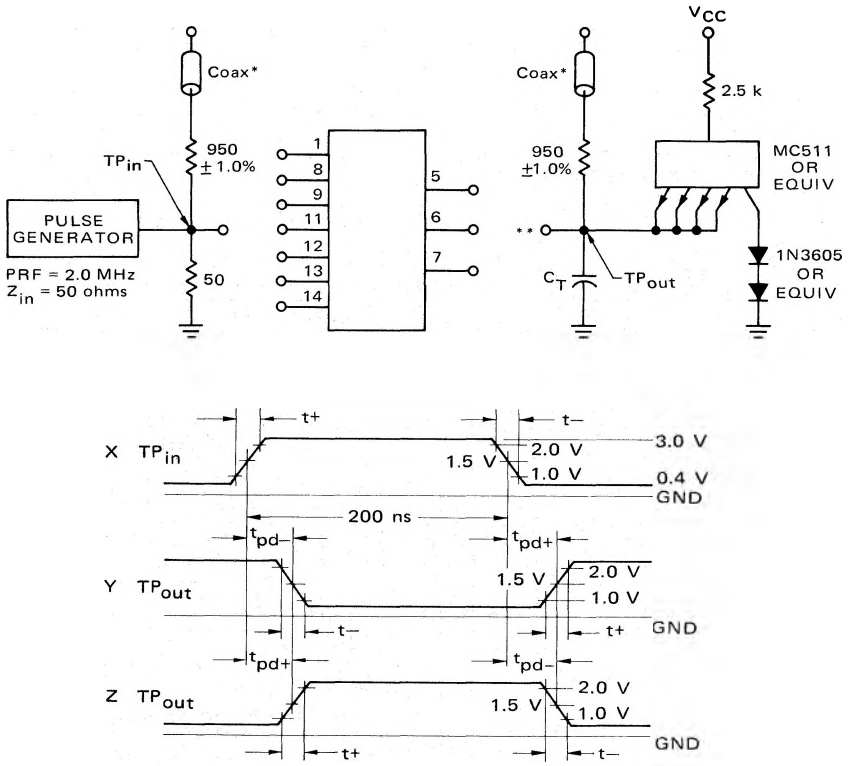
Input test procedures are shown for only inputs $\oplus_{in2}$ and A. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.

@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	V_{th1} Volts	V_{th0} Volts	V_{out} Volts	V_{max} Volts	V_{CC} Volts
MC4328*, MC4329, MC4330*, MC4331	−55°C	20	10	-2.2	-1.2	-	0.45	2.8	4.5	2.0	0.9	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	0.45	2.8	4.5	1.7	1.0	5.5	8.0	5.0
	+125°C	20	10	-2.2	-1.2	-	0.45	2.8	4.5	1.4	0.8	5.5	-	5.0
MC4028*, MC4029, MC4030*, MC4031	0°C	20	10	-2.2	-1.2	-	0.45	3.0	4.5	1.9	1.0	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	0.45	3.0	4.5	1.8	1.0	5.5	7.0	5.0
	+75°C	20	10	-2.2	-1.2	-	0.45	3.0	4.5	1.7	1.0	5.5	-	5.0

Characteristic	Symbol	Pin Under Test	MC4328 thru MC4331 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4028 thru MC4031 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}	Gnd
Input																											
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	8,9,11,12,13,14	-	-	-	-	4	1,10
		8	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAdc	-	-	-	-	-	1,9,11,12,13,14	-	-	-	-	4	8,10
Leakage Current	I_R	1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	1	-	-	-	-	4	8,9,10,11,12,13,14
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	8	-	-	-	-	4	1,9,10,11,12,13,14
Inverse Beta Current	I_L	1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	1	-	-	-	-	4	10
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	8	-	-	-	-	4	10
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	4	8,9,10,11,12,13,14
		1	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	1	-	-	-	-	-	-	-	4	10,12,14
		8	-	-		-	-	-	-	-		-	-	-		-	-	8	-	-	-	-	-	-	-	4	1,9,10,11,12,13,14
		8	-	-		-	-	-	-	-		-	-	-		-	-	8	-	-	-	-	-	-	-	4	10,12,14
Output																											
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	8,9	11,13	-	-	4	10
	V_{out} "1"	7	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	7	-	-	-	-	8,9	11,13	-	-	4	10
Leakage Current	I_{OLK}	6	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	6	-	4	8,10
Short-Circuit Current	I_{SC}	5**	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	-	4	5,10
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.45	-	0.4	-	0.4	-	0.45	Vdc	5	-	-	11,13	8,9	-	-	-	-	-	4	10
	V_{OH}	7	2.7	-	3.1	-	3.15	-	2.8	-	3.1	-	3.15	-	Vdc	-	7	-	11,13	8,9	-	-	-	-	-	4	10
Power Requirements (Total Device)																											
Maximum Power Supply Current	I_{max}	4	-	-	-	55	-	-	-	-	-	65	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	8, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	4	-	32	-	32	-	32	-	41	-	41	-	41	mAdc	-	-	-	-	-	-	-	-	-	-	4	10
	I_{PDL}	4	-	38	-	38	-	38	-	48	-	48	-	48	mAdc	-	-	-	-	-	-	-	-	-	-	4	8, 9, 10, 11, 13

*Prime Fan-Out
**Short one output at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**Load only pin 5 when testing output 5. Load both outputs 6 and 7 when testing pin 6 or 7.

SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

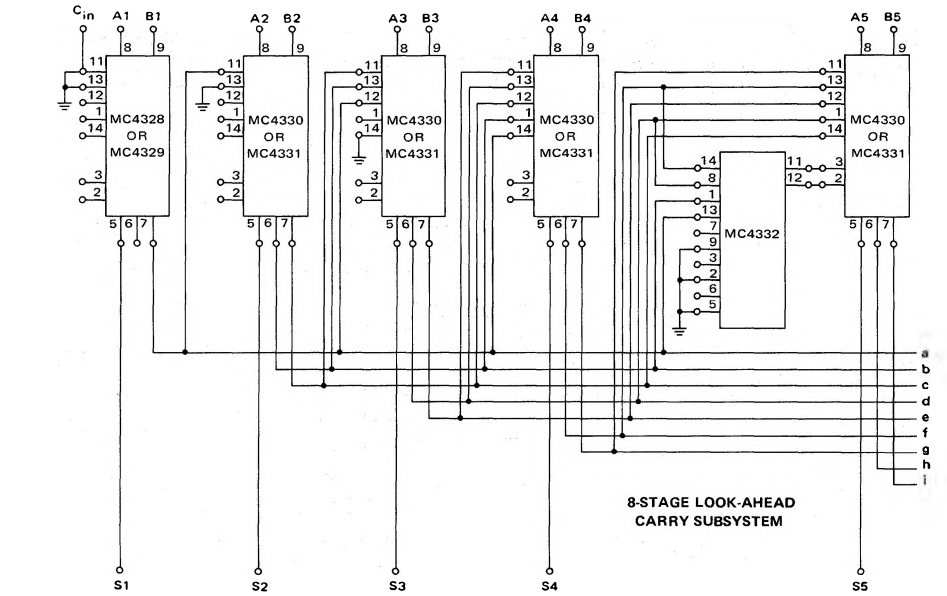
TEST	PINS UNDER TEST (In/Out)	INPUT PIN							OUTPUT PIN			LIMITS ns max
		8 A	9 B	11 C_{in1}	12 C_{in2}	13 $\oplus_{in1}$	14 C_{in3}	1 $\oplus_{in2}$	5 SUM	6 $\oplus_{out}$	7 C_{out}	
t_{pd+}	11/5	Open	Gnd	X	Open	Gnd	Open	Open	Y	–	–	35
t_{pd-}	11/5	Open	Gnd	X	Open	Gnd	Open	Open	Y	–	–	35
t_{pd+}	8/6	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	Y	–	30
t_{pd-}	8/6	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	Y	–	30
t_{pd+}	8/7	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	–	Z	20
t_{pd-}	8/7	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	–	Z	20
t+	Tested during each of the above tests.											8.0
t–												5.0

TYPICAL APPLICATION

The MC4328/29 and MC4330/31 adders can be used with the MC4332 Carry Decoder to build 8-stage look-ahead carry subsystems. Each stage examines the carry outputs from all previous stages while adding bits A and B for that stage. The carry outputs of the first and eighth stages are dependent upon the carry inputs from previous stages; thus the MC4328/29 adder is used for stages one and eight while the MC4330/31 adder is used for stages two through seven. The MC4332 Carry Decoder is used to expand the look-ahead carry input capability required for stages four through eight.

The add delay of an eight stage adder is equal to the sum of the add delay and the delay from the A and B inputs to the ⊕output of one stage. Thus the typical add delay for an 8-stage adder is 25 ns + 13 ns or 38 ns typical.

When expander inputs are not used they should not be connected to any external point. This minimizes possible problems resulting from noise pick-up.



8-STAGE LOOK-AHEAD CARRY SUBSYSTEM