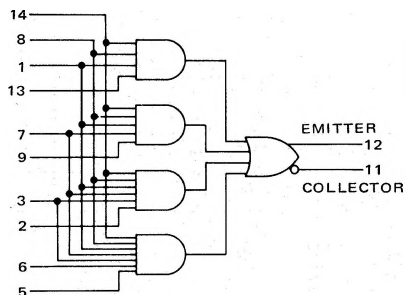


CARRY DECODER

MC4300/MC4000 series

MC4332F,L*
MC4032F,L,P*



V_{CC} = Pin 4
GND = Pin 10

This 4-wide 4, 5, 6, 7 input AND-OR expander provides the necessary logic for carry decoding between look-ahead carry adder stages using the MC4328/29 and MC4330/31 fast adders.

Input Loading Factor:

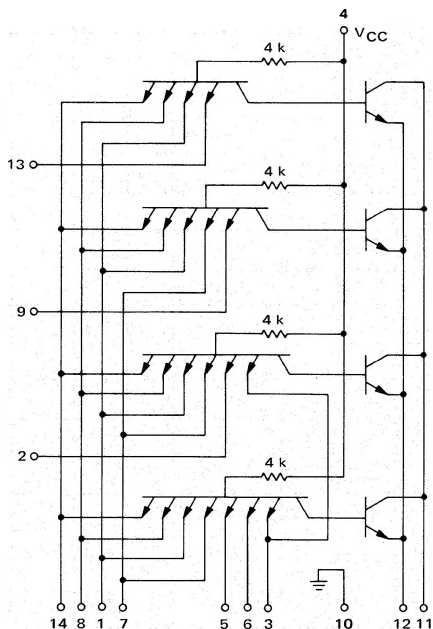
Pins 1, 8, 14 = 4
Pin 7 = 3
Pin 9 = 2
Pins 2, 5, 6, 9, 13 = 1

Total Power Dissipation = 20 mW typ/pkg

Δt_{pd} = 4.0 ns typ/decoder

1.0 ns typ/pF at expander nodes

TYPICAL APPLICATION



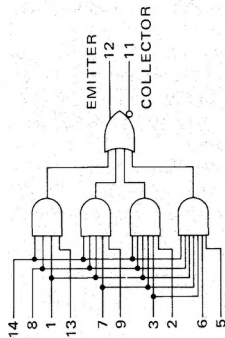
The MC4328/29 and MC4330/31 adders can be used with the MC4332 Carry Decoder to build 8-stage look-ahead carry subsystems. (See the MC4328-31) data sheet for a diagram.) Each stage examines the carry outputs from all previous stages while adding bits A and B for that stage. The carry outputs of the first and eighth stages are dependent upon the carry inputs from previous stages; thus the MC4328/29 adder is used for stages one and eight while the MC4330/31 adder is used for stages two through seven. The MC4332 Carry Decoder is used to expand the look-ahead carry input capability required for stages four through eight.

The add delay of an eight stage adder is equal to the sum of the add delay and the delay from the A and B inputs to the \oplus output of one stage. Thus the typical add delay for an 8-stage adder is 25 ns + 13 ns or 38 ns typical.

When expander inputs are not used they should not be connected to any external point. This minimizes possible problems resulting from noise pick-up.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

Test procedures are shown for only one set of inputs. Test remaining inputs in the same manner.

[illegible]

*Voltage measured between pins 11 and 12.