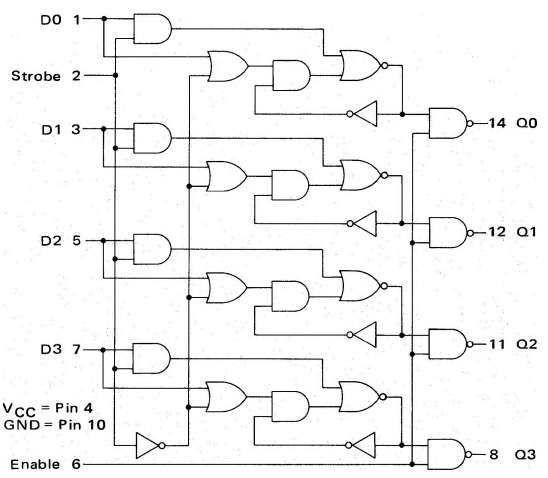
QUAD LATCH
(Open Collector)

MC4335F, L*
MC4035F, L, P*



Two 5.0 k ohm pullup resistors are internally connected to V_{CC} and brought out on pins 9 and 13.

This monolithic device consists of four latch circuits with open collector outputs, common Strobe input, and output enable input. The output of each latch will follow the data input when the Strobe input is in a logical "1" state. When the Strobe is in a logical "0" state, the latch will store the logic state of the data input just prior to the change of the Strobe from a "1" level to a "0" level.

The open collector outputs make this device useful for bussing or wire ORing outputs together. Two 5.0 k ohm resistors are available in the package to provide the passive pullup function in wired-OR or bussed operation. The output enable is useful where it is desirable to gate information out of the latches according to a predetermined timing scheme.

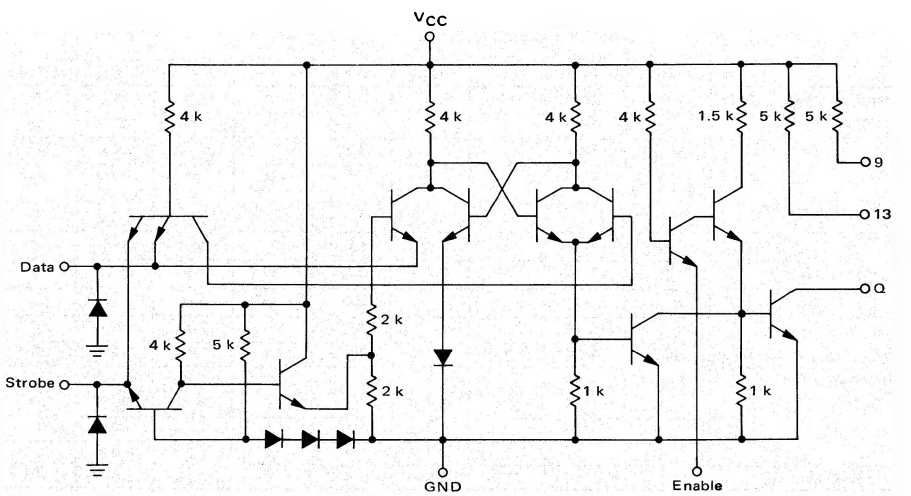
Input Loading Factor (MTTL I Loads):
- Data Input (Strobe High) — MC4335 = 4.2, MC4035 = 4.0
- Data Input (Strobe Low) — MC4335 = 1.1, MC4035 = 0.9
- Output Enable — MC4335 = 4.0, MC4035 = 3.6
- Strobe — MC4335 = 5.2, MC4035 = 5.2

Output Loading Factor (MTTL I Loads):
- MC4335 = 7 (I_{OL} = 9.3 mAdc)
- MC4035 = 7 (I_{OL} = 11.6 mAdc)

Total Power Dissipation = 140 mW typ/pkg
Propagation Delay Time = 25 ns typ

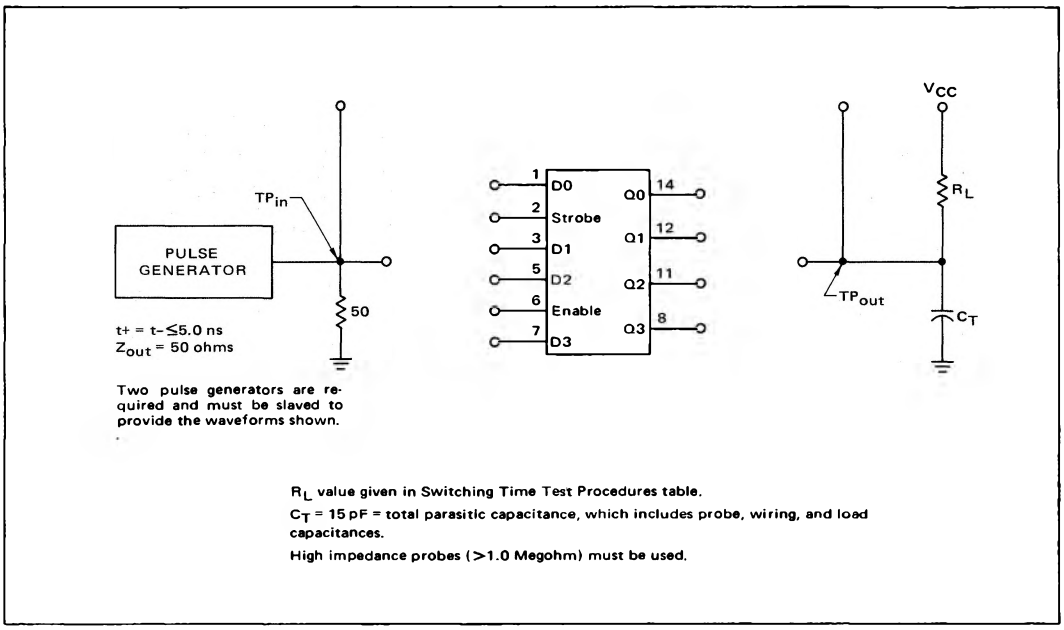
CIRCUIT SCHEMATIC

1/4 OF DEVICE SHOWN



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

SWITCHING TIME TEST CIRCUIT



R_L value given in Switching Time Test Procedures table.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 Megohm) must be used.

SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

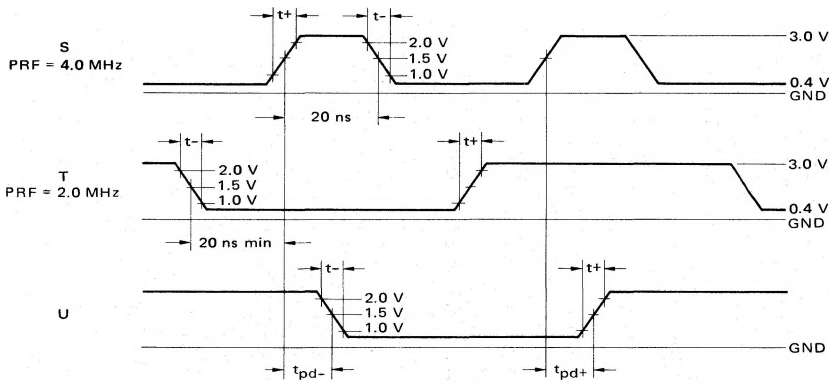
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST (In/Out)	INPUT Pin 1 D0	INPUT Pin 2 Strobe	INPUT Pin 6 Enable	OUTPUT Pin 14 D0	R_L Ohms MC4335	R_L Ohms MC4035	LIMITS (ns) Max MC4335	LIMITS (ns) Max MC4035
Strobe Propagation Delay	t_{pd+1}	2/14	T	S	2.4 V	U	510	390	25	25
	t_{pd-1}	2/14	T	S	2.4 V	U	510	390	40	35
	t_{pd+2}	2/14	T	S	2.4 V	U	5.0 k	5.0 k	50	50
	t_{pd-2}	2/14	T	S	2.4 V	U	5.0 k	5.0 k	34	34
Rise Time	t+	14	T	S	2.4 V	U	510 or 5.0 k	390 or 5.0 k	0.3 RC	0.3 RC
Fall Time	t-	14	T	S	2.4 V	U	510	390	9.0	5.0
Data Propagation Delay	t_{pd+3}	1/14	V	2.4 V	2.4 V	W	510	390	20	20
	t_{pd-3}	1/14	V	2.4 V	2.4 V	W	510	390	30	25
	t_{pd+4}	1/14	V	2.4 V	2.4 V	W	5.0 k	5.0 k	50	50
	t_{pd-4}	1/14	V	2.4 V	2.4 V	W	5.0 k	5.0 k	25	25
Enable Propagation Delay	t_{pd+3}	1/14	X	2.4 V	Y	Z	510	390	20	20
	t_{pd-3}	1/14	X	2.4 V	Y	Z	510	390	30	25
	t_{pd+4}	1/14	X	2.4 V	Y	Z	5.0 k	5.0 k	50	50
	t_{pd-4}	1/14	X	2.4 V	Y	Z	5.0 k	5.0 k	25	25
Minimum Strobe Enable	–	1/14	T ①	1.8 V	2.4 V	②	5.0 k	5.0 k	②	②
Maximum Strobe Inhibit	–	1/14	T ①	1.0 V	2.4 V	③	5.0 k	5.0 k	③	③

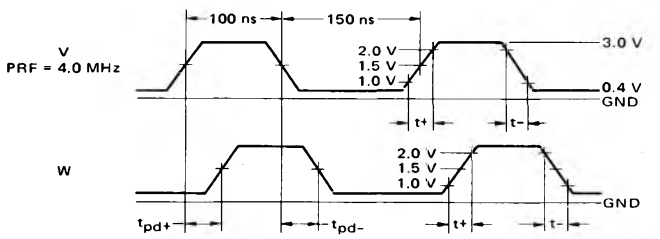
① Pulse T conditions changed: V_L = 1.0 V, V_H = 1.8 V
② Output shall follow data input.
③ Output shall not toggle.

VOLTAGE WAVEFORMS

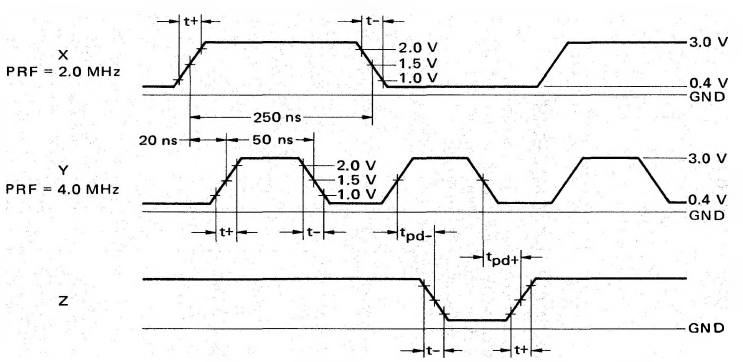
STROBE INPUT



DATA INPUTS

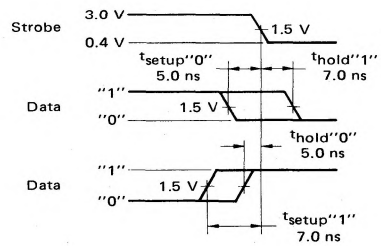


ENABLE INPUT



OPERATING CHARACTERISTICS

This quad latch consists of four gated latches that store data on the negative edge of the strobe input. Information must be present at the data inputs prior to the setup time and remain at the data inputs through the hold time to insure that it will be stored by the latch when the negative edge of the strobe occurs. The setup time is 7.0 ns for a logical "1" and 5.0 ns for a logical "0". Hold time is 7.0 ns after the strobe edge for a logical "1" and 5.0 ns prior to the strobe edge for a logical "0".



ELECTRICAL CHARACTERISTICS

Test procedures are shown for the Strobe, Enable, and only one data input, and for one output. Other data inputs and outputs are tested in the same manner.

																	TEST CURRENT/VOLTAGE VALUES (All Temperatures)															
																	mA			Volts												
																	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}				
																MC4335	11.6	0.1	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.5	5.5				
																MC4035	9.3	0.1	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.75	5.25				
			MC4335 Test Limits						MC4035 Test Limits								TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																
		Pin	−55°C		+25°C		+125°C		0°C		+25°C		+75°C																		Pulse	Pulse	
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	1	2	Gnd
Input																																
Forward Current	I_F	1	-	-5.6	-	-5.6	-	-5.6	-	-6.7	-	-6.7	-	-6.7	mAdc	-	-	-	-	-	1	2	-	-	-	-	4	-	-	10
		1	-	-1.5	-	-1.5	-	-1.5	-	-1.8	-	-1.8	-	-1.8		-	-	-	2	-	1	3,5,7	-	-	-	-		-	-	
		2	-	-7.0	-	-7.0	-	-7.0	-	-8.6	-	-8.6	-	-8.6		-	-	-	-	-	2	1,3,5,6,7	-	-	-	-		-	-	
		6	-	-5.3	-	-5.3	-	-5.3	-	-6.0	-	-6.0	-	-6.0		-	-	-	-	-	6	1,2,3,5,7	-	-	-	-		-	-	
		13	-	-1.3	-	-1.3	-	-1.3	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	13	1	-	-	-	-		-	-	
Leakage Current	I_R	1	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	1	-	-	-	-	4	-	-	2,10
		2	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5		-	-	-	-	-	-	2	-	-	-	-		-	-	1,3,5,7,10
		6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4		-	-	-	-	-	-	6	-	-	-	-		-	-	1,2,3,5,7,10
Breakdown Voltage	BV_{in}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,10
		2		-		-		-		-		-		-		-	-	2	-	-	-	-	-	-	-	-		-	-	1,3,5,6,7,10
		6		-		-		-		-		-		-		-	-	6	-	-	-	-	-	-	-	-		-	-	1,2,3,5,7,10
Output																																
Output Voltage	V_{OL}	14	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	14	-	-	-	6	-	2,3,5,7	-	-	-	4	-	-	-	1,10
		14	-		-		-		-		-		-			14	-	-	1	2,6	-	-	-	-	-		-	-	-	10
		14	-		-		-		-		-		-			14	-	-	-	-	-	-	-	-	-		-	2	1	10
	V_{OH}	14	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	14	-	6	-	-	2	-	-	-	4	-	-	-	1,3,5,7,10
		14	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	14	-	-	1,2,6	-	-	-	-	-	4	-	-	-	10
Leakage Current	I_{CEX}	14	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	1,2	14	-	-	-	4	-	-	10
		14	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	mAdc	-	-	-	-	-	-	-	-	14	4	-	-	-	-	6,10
Power Requirements (Total Device)																																
Maximum Power Supply Current	I_{max}	4	-	-	-	44	-	-	-	-	-	52	-	-	mAdc	-	-	-	-	-	-	2	-	4	-	-	-	-	-	1,3,5,6,7,10
Power Supply Drain	I_{PDH}	4	-	42	-	42	-	42	-	50	-	50	-	50	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	10
	I_{PDL}	4	-	34	-	34	-	34	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	1,3,5,6,7,10