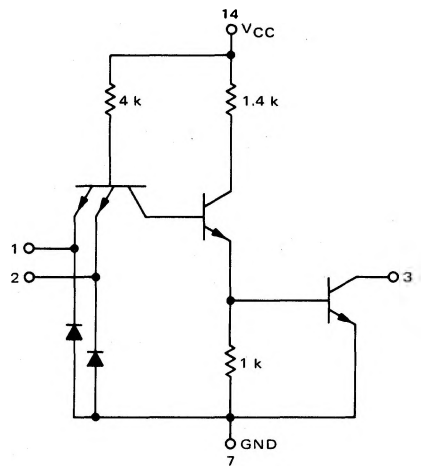
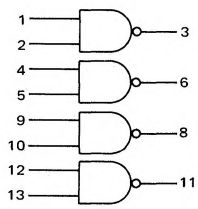
QUAD 2-INPUT INTERFACE
"NAND" GATE

MC5426L*
MC7426P,L*

1/4 OF CIRCUIT SHOWN



This device features high-output voltage ratings for use as an interface circuit with 12 volt systems, such as low threshold voltage MOS logic circuits. The output is rated at 15 volts, however, V_{CC} is connected to the standard 5 volt source. The output transistor has a 16 milliamp sink capability at an output voltage of 0.4 volt maximum, thus allowing high fan-out drive capability while maintaining the nominal power dissipation of the standard gate.



Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$

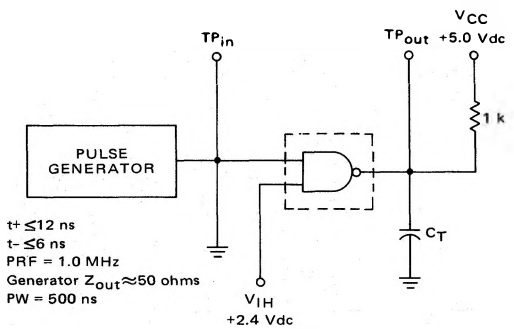
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg

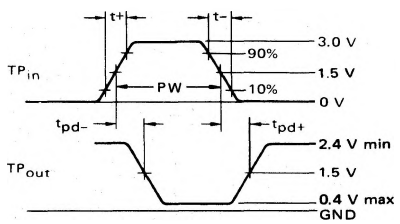
Propagation Delay Time = 17 ns typ

*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST CIRCUIT

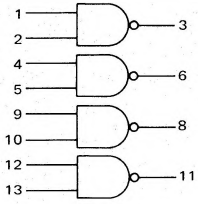


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
									mA		Volts										
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	$V_{th\ 1}$	$V_{th\ 0}$	V_{OH}	V_{CC}	V_{CCL}	V_{CCH}	
								MC5426	16	1	0.4	2.4	4.5	5.5	2.0	0.8	12	5.0	4.5	5.5	
								MC7426	16	1	0.4	2.4	4.5	5.5	2.0	0.8	12	5.0	4.75	5.25	
			MC5426 Test Limits -55 to +125°C			MC7426 Test Limits 0 to 70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	$V_{th\ 1}$	$V_{th\ 0}$	V_{OH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	1	–	2	–	–	–	–	–	–	14	7*
Leakage Current	I_{R1}	1	–	40	µAdc	–	40	µAdc	–	–	–	1	–	–	–	–	–	–	–	14	2,7*
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	–	–	14	2,7*
Output																					
Output Voltage	V_{OL}	3	–	0.4	Vdc	–	0.4	Vdc	3	–	–	–	–	–	1,2	–	–	–	14	–	7*
	V_{OH}	3	15	–	Vdc	15	–	Vdc	–	3	–	–	–	–	–	2	–	–	1,14	–	7*
Output Current	I_{OH}	3	–	50	µAdc	–	50	µAdc	–	–	–	–	–	–	–	2	3	–	1,14	–	7*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	14	–	22	mAdc	–	22	mAdc	–	–	–	–	–	–	–	–	–	12	–	14	7
	I_{PDL}	14	–	8.0	mAdc	–	8.0	mAdc	–	–	–	–	–	–	–	–	–	–	–	14	1,4,7,9,12
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	–	17**	ns	–	17**	ns	1	3	–	2	–	–	–	–	–	14	–	–	7
Turn-Off Delay	t_{pd+}	1,3	–	24**	ns	–	24**	ns	1	3	–	2	–	–	–	–	–	14	–	–	7

*Ground inputs to gates not under test.
**Tested only at 25°C.