BCD-TO-DECIMAL DECODER

MC5442L* • MC7442L,P*

EXCESS THREE-TO-DECIMAL DECODER

MC5443L* • MC7443L,P*

EXCESS THREE GRAY-TO-DECIMAL DECODER

MC5444L* • MC7444L,P*

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 140 mW typ/pkg

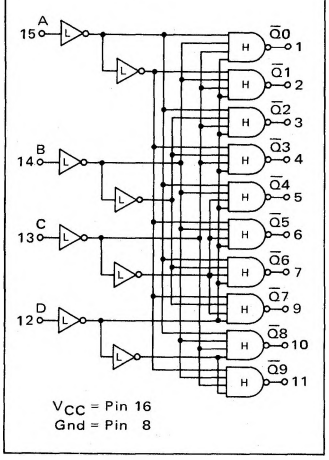
Propagation Delay Time:
2 Logic Levels = 22 ns typ
3 Logic Levels = 23 ns typ

DC Noise Margin = 1.0 V typ

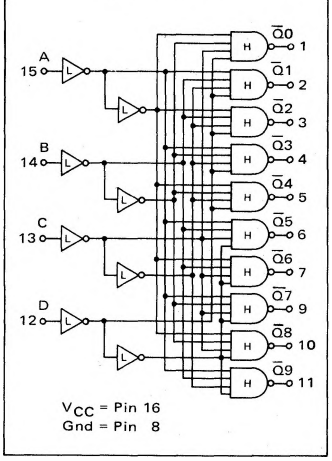
These devices decode four-bit BCD, Excess 3, or Excess 3 Gray inputs to select one-of-ten outputs. The selected output is in the logic "0" state, while all other outputs are in the logic "1" state. Full decoding of all valid input logic ensures that outputs remain off for any invalid input condition.

These devices are useful in memory selection, industrial control, and data routing applications.

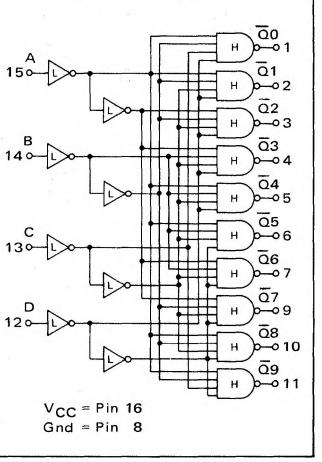
MC5442/MC7442



MC5443/MC7443



MC5444/MC7444



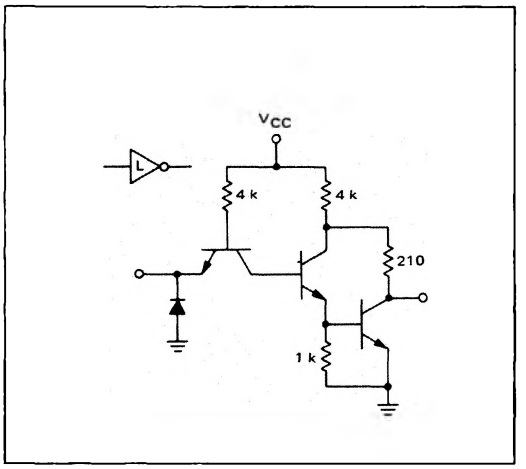
These decoders are constructed using low-level inverters and high-level NAND gates interconnected as shown by the logic diagrams. The inverter and gate schematics appear on the next page of this data sheet.

MC5442/MC7442 BCD INPUT				MC5443/MC7443 EXCESS 3 INPUT				MC5444/MC7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	0	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1

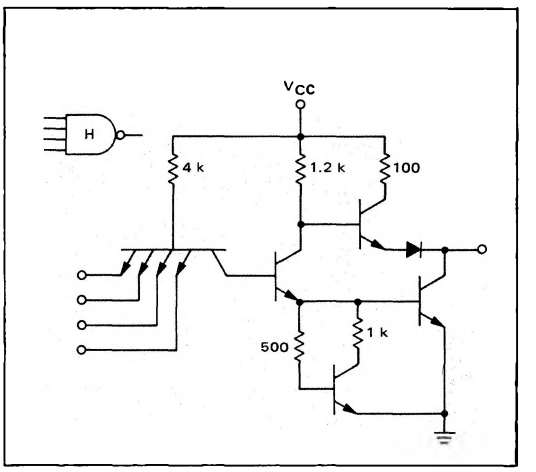
*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

CIRCUIT SCHEMATICS

LOW-LEVEL INVERTER



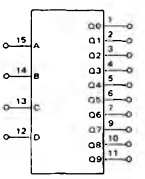
HIGH-LEVEL "NAND" GATE



MC5442/MC7442

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
MC5442	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	
MC7442	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	

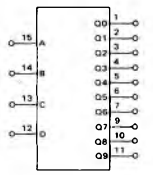
Characteristic	Symbol	Pin Under Test	MC5442 Test Limits -55 to +125°C			MC7442 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																			
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	8
Leakage Current	I_R	12	–	40	µAdc	–	40	µAdc	–	–	–	–	12	–	–	–	–	16	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	8
Output																			
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	–	12,13,14,15	–	16	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	15	12,13,14	–	16	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	12,14	13,15	–	–	16	1,8
Power Requirements (Total Device)																			
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out									
Two Logic Levels																			
Turn-On Delay	t_{pd-2}	15,1	10*	30*	ns	10*	30*	ns	15	1	–	–	–	–	–	16	–	–	8,12,13,14
Turn-Off Delay	t_{pd+2}	15,1	10*	25*	ns	10*	25*	ns	15	1	–	–	–	–	–	16	–	–	8,12,13,14
Three Logic Levels																			
Turn-On Delay	t_{pd-3}	15,2	–	35*	ns	–	35*	ns	15	2	–	–	–	–	–	16	–	–	8,12,13,14
Turn-Off Delay	t_{pd+3}	15,2	–	35*	ns	–	35*	ns	15	2	–	–	–	–	–	16	–	–	8,12,13,14

*Tested only at 25°C.

MC5443/MC7443

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC5443	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	2.5
MC7443	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	2.5

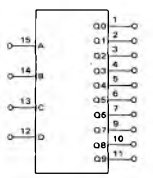
Characteristic	Symbol	Pin Under Test	MC5443 Test Limits -55 to +125°C			MC7443 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																				
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	–	8
Leakage Current	I_R	12	–	40	µAdc	–	40	µAdc	–	–	–	–	12	–	–	–	–	16	–	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	–	8
Output																				
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	14,15	12,13	–	16	–	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	13	12,14,15	–	16	–	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	12,13,14	15	–	–	16	–	1,8
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out										
Two Logic Levels Turn-On Delay	t_{pd-2}	15,2	10*	30*	ns	10*	30*	ns	15	2	–	–	–	–	–	16	–	–	13	8,12,14
Turn-Off Delay	t_{pd+2}	15,2	10*	25*	ns	10*	25*	ns	15	2	–	–	–	–	–	16	–	–	13	8,12,14
Three Logic Levels Turn-On Delay	t_{pd-3}	15,3	–	35*	ns	–	35*	ns	15	3	–	–	–	–	–	16	–	–	13	8,12,14
Turn-Off Delay	t_{pd+3}	15,3	–	35*	ns	–	35*	ns	15	3	–	–	–	–	–	16	–	–	13	8,12,14

*Tested only at 25°C.

MC5444/MC7444

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.

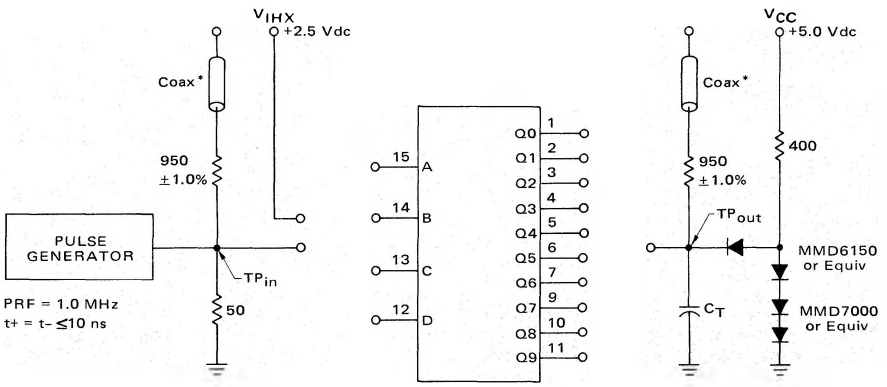


	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC5444	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	2.5
MC7444	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	2.5

Characteristic	Symbol	Pin Under Test	MC5444 Test Limits -55 to +125°C			MC7444 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																				
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	–	8
Leakage Current	I_R	12	–	40	µAdc	–	40	µAdc	–	–	–	–	12	–	–	–	–	16	–	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	–	8
Output																				
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	14	12,13,15	–	16	–	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	13,14	12,15	–	16	–	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	12,13,14,15	–	–	16	–	1,8
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out										
Two Logic Levels Turn-On Delay	t_{pd-2}	13,1	10*	30*	ns	10*	30*	ns	13	1	–	–	–	–	–	16	–	–	14	8,12,15
Turn-Off Delay	t_{pd+2}	13,1	10*	25*	ns	10*	25*	ns	13	1	–	–	–	–	–	16	–	–	14	8,12,15
Three Logic Levels Turn-On Delay	t_{pd-3}	13,2	–	35*	ns	–	35*	ns	13	2	–	–	–	–	–	16	–	–	14	8,12,15
Turn-Off Delay	t_{pd+3}	13,2	–	35*	ns	–	35*	ns	13	2	–	–	–	–	–	16	–	–	14	8,12,15

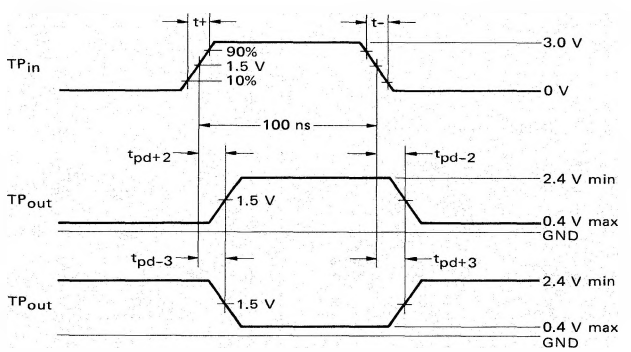
*Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



TYPICAL APPLICATIONS

Two MC5442/7442 decoders may be used to perform 4-line to 16-line decoding. Data inputs A, B, and C are paralleled to the two decoders, while input D is applied to one decoder and $\overline{D}$ to the other. (See Figure 1.)

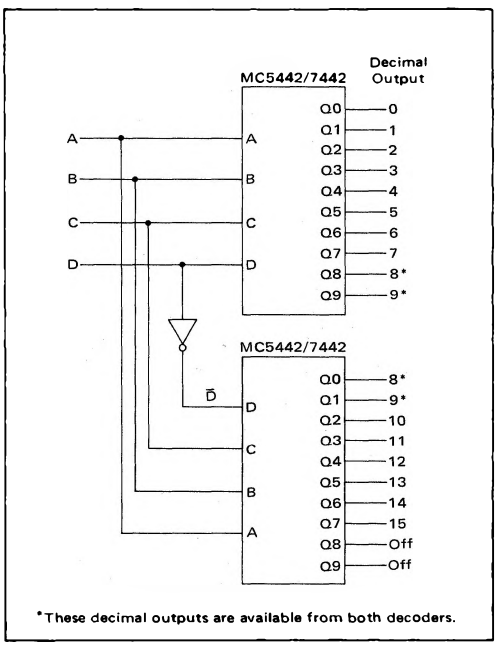
The excess 3 code is similar to the BCD code except that 3 is added to each digit before coding. This code has the advantage of being self-complementing. If all zeros in a BCD number are changed to ones and all ones are changed to zeros, the nines complement of the decimal number is obtained. The ability to obtain the nines complement can reduce the hardware necessary to perform subtraction. (See Figure 2.)

All Gray codes have one basic characteristic in common. As the code is advanced from any number to the next, only one bit of the code will change at a time. When a non-Gray code such as straight binary is advanced from 3 to 4 (0011 to 0100) three bits of the code must change. Since in many applications the voltages on the three lines do not change simultaneously, a number of false outputs may be generated which last for a short time. These false outputs are easily accepted by the high-speed devices now in use. In contrast, the excess 3 Gray code of the MC5444/7444 would change from 0101 to 0100 to advance from 3 to 4.

Analog measuring devices require a converter for information fed to a digital system. These converters usually use a Gray code output. Gray codes are also useful in sequential circuitry because of the change of only one bit at a time.

Figure 3 shows the MC5444/7444 used for decoding 3-line binary-to-octal. The input to A, B, and D is the binary code ABC. The C input of the device is used as a strobe. Octal data is taken from outputs Q1 through Q8 when the strobe is taken to a logic "1". Outputs Q0 and Q9 are not used.

FIGURE 1 – BINARY-TO-DECIMAL DECODING USING MC5442/7442



*These decimal outputs are available from both decoders.

FIGURE 2 – 4-LINE EXCESS THREE CODE-TO-NINES COMPLEMENT DECIMAL DECODING USING MC5443/7443

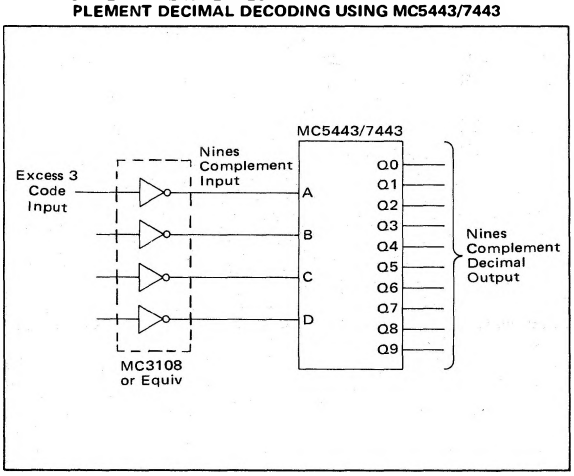


FIGURE 3 – 3-LINE BINARY-TO-OCTAL DECODING USING MC5444/7444