GATED FULL ADDER

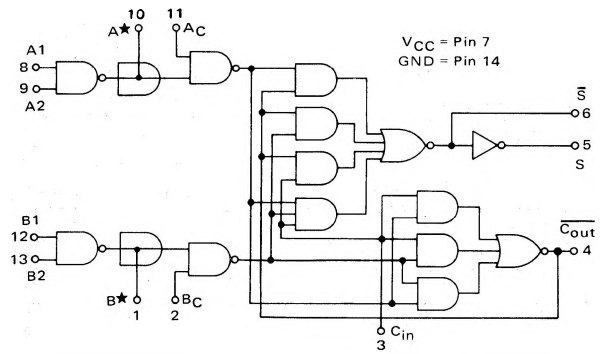
MC5480L*
MC7480L, P*

The MC5480/7480 is a one-bit binary full adder with gated complementary inputs, complementary Sum and $\overline{\text{Sum}}$ outputs, and an inverted Carry output. The circuit uses DTL inputs and a high-speed, high-fan-out, TTL "totem pole" configuration for the Sum, $\overline{\text{Sum}}$, and Carry outputs. The design of the high-speed carry circuitry reduces the need for external "look ahead carry" cascading in system designs. The use of low-level, low-power gates in a monolithic design provides significantly lower power dissipation than equivalent adders built from standard integrated circuits.

This full adder provides a basic building block for medium and high-speed, multiple-bit, parallel-add/serial-carry subsystems.

TRUTH TABLE

C_{in}	B	A	$\overline{C_{out}}$	$\overline{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

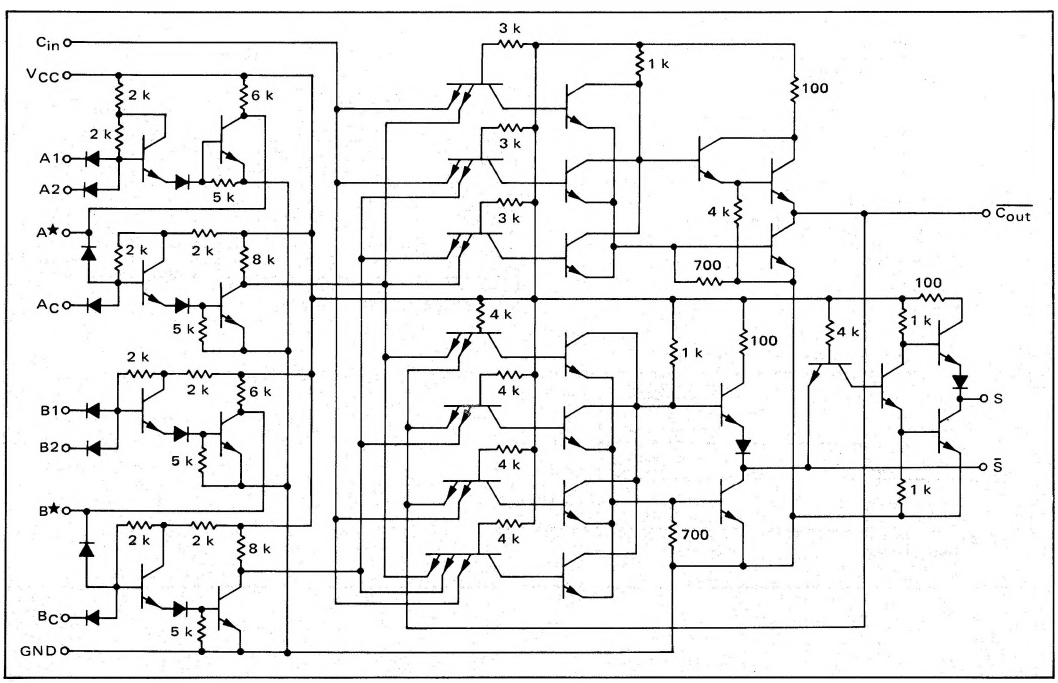


Input Loading Factor:
A1, A2, A_C, B1, B2, B_C = 1
A★, B★ = 1.625
C_{in} = 5

Output Loading Factor:
$\overline{C_{out}}$ = 5
S, $\overline{S}$ = 10
A★, B★ = 3

1. $A = \overline{A★ \cdot A_C}$, $B = \overline{B★ \cdot B_C}$
   where $A★ = \overline{A_1 \cdot A_2}$
   $B★ = \overline{B_1 \cdot B_2}$
2. When A★ (or B★) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
3. When A1 and A2 (or B1 and B2) are used as inputs, A★ (or B★) must be open, or used to perform wired-OR logic.

Total Power Dissipation = 105 mW typ/pkg
Propagation Delay Time:
Carry Delay = 10 ns typ
Add Delay = 55 ns typ



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Output voltage (logic level) tests are shown only for each output. The complete circuit can be tested by following the truth table.

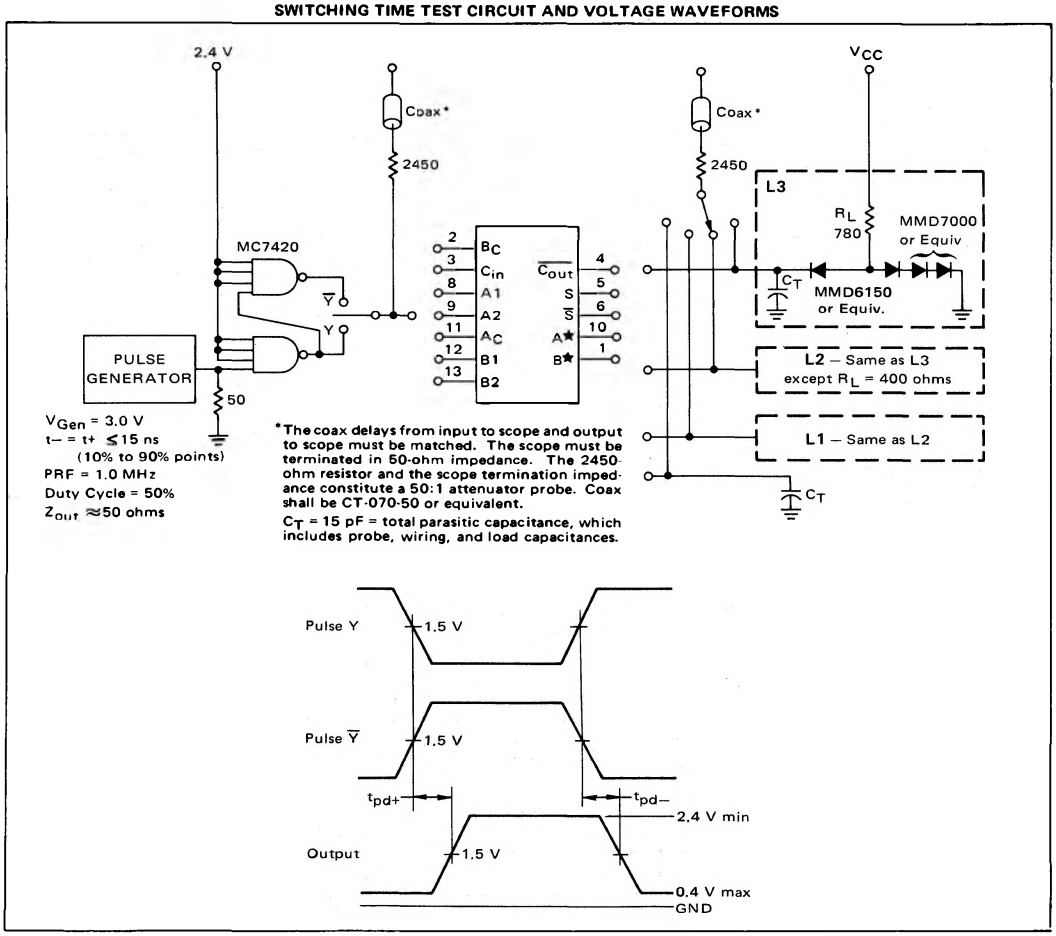
	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA						Volts							
	I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}
MC5480	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
MC7480	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5480 Test Limits −55 to +125°C Min	Max	Unit	MC7480 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current B✱	I_F	1	-	-2.6	mAdc	-	-2.6	mAdc	-	-	-	-	-	-	1	-	-	2	-	-	-	14	7, 12, 13
B_C		2	-	-1.6		-	-1.6		-	-	-	-	-	-	2	-	-	-	-	-	-		7, 12, 13
C_{in}		3	-	-8.0		-	-8.0		-	-	-	-	-	-	3	-	-	-	-	-	-		7
A1		8	-	-1.6		-	-1.6		-	-	-	-	-	-	8	-	-	9	-	-	-		
A2		9	-	-1.6		-	-1.6		-	-	-	-	-	-	9	-	-	8	-	-	-		
A✱		10	-	-2.6		-	-2.6		-	-	-	-	-	-	10	-	-	11	-	-	-		7, 8, 9
A_C		11	-	-1.6		-	-1.6		-	-	-	-	-	-	11	-	-	-	-	-	-		7, 8, 9
B1		12	-	↓	↓	-	↓	↓	-	-	-	-	-	-	12	-	-	13	-	-	-		7
B2		13	-	↓	↓	-	↓	↓	-	-	-	-	-	-	13	-	-	12	-	-	-	↓	7
Leakage Current B_C	I_{R1}	2	-	15	μAdc	-	15	μAdc	-	-	-	-	-	-	-	2	-	-	-	-	-	14	1, 7
C_{in}		3	-	200		-	200		-	-	-	-	-	-	-	3	-	-	-	-	-		7, 8, 9, 12, 13
A1		8	-	15		-	15		-	-	-	-	-	-	-	8	-	-	-	-	-		7, 9
A2		9	-	↓		-	↓		-	-	-	-	-	-	-	9	-	-	-	-	-		7, 8
A_C		11	-			-			-	-	-	-	-	-	-	11	-	-	-	-	-		7, 10
B1		12	-			-			-	-	-	-	-	-	-	12	-	-	-	-	-		7, 13
B2		13	-	↓	↓	-	↓	↓	-	-	-	-	-	-	-	13	-	-	-	-	-	↓	7, 12
B_C	I_{R2}	2	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	-	-	-	-	2	-	-	-	-	14	1, 7
C_{in}		3	-			-			-	-	-	-	-	-	-	-	3	-	-	-	-		7, 8, 9, 12, 13
A1		8	-			-			-	-	-	-	-	-	-	-	8	-	-	-	-		7, 9
A2		9	-			-			-	-	-	-	-	-	-	-	9	-	-	-	-		7, 8
A_C		11	-			-			-	-	-	-	-	-	-	-	11	-	-	-	-		7, 10
B1		12	-			-			-	-	-	-	-	-	-	-	12	-	-	-	-		7, 13
B2		13	-	↓	↓	-	↓	↓	-	-	-	-	-	-	-	-	13	-	-	-	-	↓	7, 12
Output																							
Output Voltage A✱	V_{OL}	1	-	0.4	Vdc	-	0.4	Vdc	1	-	-	-	-	-	-	-	-	-	12, 13	-	14	-	7
$\overline{C}_{out}$		4	-			-			-	4	-	-	-	-	-	-	-	-	8, 12	2,3,9,11,13		-	
S		5	-			-			-	-	5	-	-	-	-	-	-	-	2, 11	3,8,9,12,13		-	
$\overline{S}$		6	-	↓	↓	-	↓	↓	-	-	6	-	-	-	-	-	-	-	2,3,8,11,12	9, 13	↓	-	↓
B✱		10	-			-			10	-	-	-	-	-	-	-	-	-	8, 9	-		-	
A✱	V_{OH}	1	2.4	-	Vdc	2.4	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	12,13	14	-	7
$\overline{C}_{out}$		4		-			-		-	-	-	-	4	-	-	-	-	-	2, 11	3,8,9,12,13		-	
S		5		-			-		-	-	-	-	-	5	-	-	-	-	2, 9, 13	3,8,11,12		-	
$\overline{S}$		6		-			-		-	-	-	-	-	6	-	-	-	-	3, 10, 11	1,2,8,9,12,13		-	
B✱		10	↓	-	↓	↓	-	↓	-	-	-	10	-	-	-	-	-	-	-	8, 9	↓	-	↓
Short-Circuit Current	I_{SC}																						
$\overline{C}_{out}$		4	-20	-70	mAdc	-18	-70	mAdc	-	-	-	-	-	-	-	-	-	2,3,8,11,12	-	-	-	14	4,7,9,13
S		5	↓	-57	↓	↓	-57	↓	-	-	-	-	-	-	-	-	-	2,9,13	-	-	-	↓	3,5,7,8,11,12
$\overline{S}$		6		-57			-57		-	-	-	-	-	-	-	-	-	3,10,13	-	-	-		1,2,6,7,8,9,12,13
Power Requirements																							
Power Supply Drain	I_{PD}	14	-	31**	mAdc		35**	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	7

**Tested only at 25°C.

MC5480L, MC7480L, P (continued)

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



TEST PROCEDURES (T_A = 25°C)

TEST	PIN UNDER TEST	INPUT B_C Pin 2	C_{in} Pin 3	A1 Pin 8	A2 Pin 9	A_C Pin 11	B1 Pin 12	B2 Pin 13	OUTPUT $\overline{C_{out}}$ Pin 4	S Pin 5	$\overline{S}$ Pin 6	A★ Pin 10	B★ Pin 1	MAX LIMIT
t_{pd+} $\overline{C_{out}}$	4	–	Y	–	–	–	Gnd	–	L3	–	–	–	–	17 ns
t_{pd-} $\overline{C_{out}}$	4	–	Y	–	–	–	Gnd	–	L3	–	–	–	–	12 ns
t_{pd+} $\overline{C_{out}}$	4	$\overline{Y}$	2.4 V	Gnd	–	–	Gnd	–	L3	–	–	–	–	25 ns
t_{pd-} $\overline{C_{out}}$	4	$\overline{Y}$	2.4 V	Gnd	–	–	Gnd	–	L3	–	–	–	–	55 ns
t_{pd+} S	5	–	2.4 V	Gnd	–	$\overline{Y}$	Gnd	–	L3	L1	L2	–	–	70 ns
t_{pd-} S	5	–	2.4 V	Gnd	–	$\overline{Y}$	Gnd	–	L3	L1	L2	–	–	80 ns
t_{pd+} $\overline{S}$	6	$\overline{Y}$	2.4 V	–	–	–	Gnd	–	–	–	L2	–	–	55 ns
t_{pd-} $\overline{S}$	6	$\overline{Y}$	2.4 V	–	–	–	Gnd	–	–	–	L2	–	–	75 ns
t_{pd+} A★	10	–	–	Y	2.4 V	–	–	–	–	–	–	C_T	–	65 ns
t_{pd-} A★	10	–	–	Y	2.4 V	–	–	–	–	–	–	C_T	–	25 ns
t_{pd+} B★	1	–	–	–	–	–	Y	2.4 V	–	–	–	–	C_T	65 ns
t_{pd-} B★	1	–	–	–	–	–	Y	2.4 V	–	–	–	–	C_T	25 ns