DECADE COUNTER

MC5490F,L*
MC7490F,L,P*

This 4-bit counter is comprised of a divide-by-two section and a divide-by-five section. These sections can be used independently, or can be connected to perform the counting function or the simple divide-by-ten function with an output duty cycle of 50%. Two sets of direct RESET inputs are provided to allow setting all outputs to a logic "0" or to the BCD count of 9.

RESET/COUNT TRUTH TABLE

R0		R9		OUTPUT			
Pin 2	Pin 3	Pin 6	Pin 7	Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

X = Don't care.

COUNT SEQUENCE TRUTH TABLE

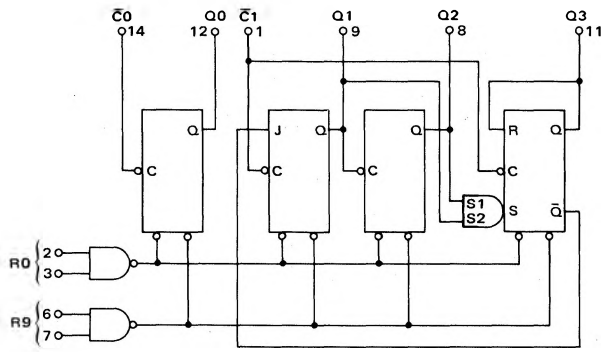
COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to $\overline{C}1$.

Input Loading Factor:
R0, R9 = 1
$\overline{C}0$ = 2
$\overline{C}1$ = 4

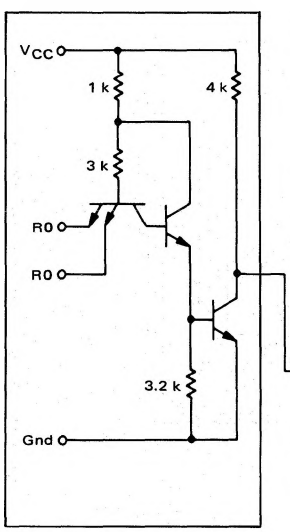
Output Loading Factor = 10

Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 20 ns typ/bit

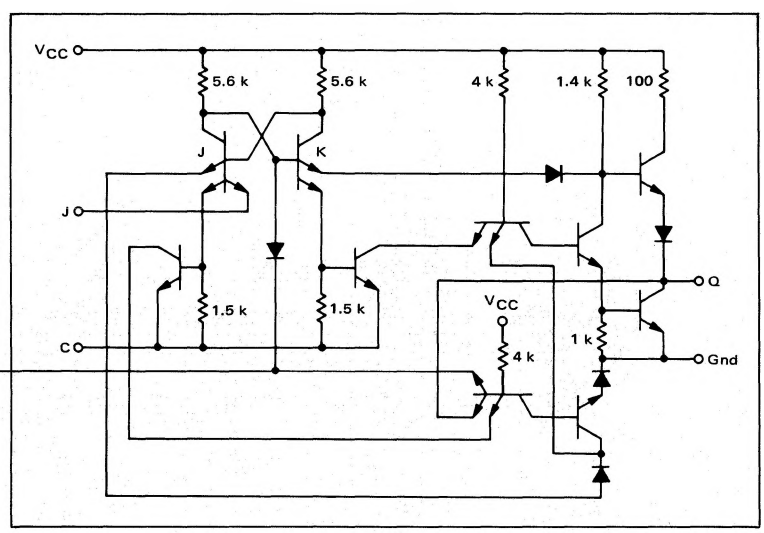


V_{CC} = Pin 5
GND = Pin 10

TYPICAL RESET GATE



TYPICAL FLIP-FLOP



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of each reset gate. The other input of each reset gate is tested in the same manner.

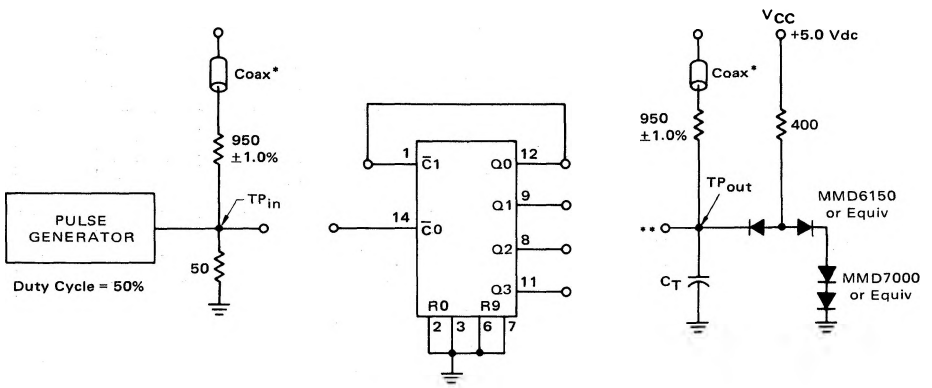
	TEST CURRENT / VOLTAGE VALUES (All Temperatures)													
	mA		Volts											
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\,1}$	$V_{th\,0}$	$V_{th\,L}$	V_{CC}	V_{CCL}	V_{CCH}		
MC5490	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.7	5.0	4.5	5.5		
MC7490	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.8	5.0	4.75	5.25		

Characteristic		Symbol	Pin Under Test	MC5490 Test Limits −55 to +125°C Min	Max	Unit	MC7490 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\,1}$	$V_{th\,0}$	$V_{th\,L}$	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																						
Forward Current	R0	I_F	2	-	-1.6	mAdc	-	-1.6	mAdc	-	-	2	-	-	3	-	-	-	-	-	5	-	10
	R9		6	-	-1.6	↓	-	-1.6	↓	-	-	6	-	-	7	-	-	-	-	-	↓	-	10
	$\overline{C}0$		14	-	-3.2		-	-3.2		-	-	14	-	-	-	-	-	-	-	-		-	2,10
	$\overline{C}1$		1	-	-6.4		-	-6.4		-	-	1	-	-	-	-	-	-	-	-		-	2,10
Leakage Current	R0	I_{R1}	2	-	40	μAdc	-	40	μAdc	-	-	-	2	-	-	-	-	-	-	-	5	-	3,10
	R9		6	-	40	↓	-	40	↓	-	-	-	6	-	-	-	-	-	-	-	↓	-	7,10
	$\overline{C}0$		14	-	80		-	80		-	-	-	14	-	-	-	-	-	-	-		-	10
	$\overline{C}1$		1	-	160		-	160		-	-	-	1	-	-	-	-	-	-	-		-	10
	R0	I_{R2}	2	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	2	-	-	-	-	-	-	5	-	3,10
	R9		6	-	↓	↓	-	↓	↓	-	-	-	-	6	-	-	-	-	-	-	↓	-	7,10
	$\overline{C}0$		14	-			-			-	-	-	-	14	-	-	-	-	-	-		-	10
	$\overline{C}1$		1	-			-			-	-	-	-	1	-	-	-	-	-	-		-	10
Output																						
Output Voltage	Q0 ①	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	2,3,14	6,7	-	-	5	-	-	10
Short-Circuit Current		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	2,3,6,7	14	-	-	5	14	10,12
Output Voltage		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	-	-	2,3,6,7,14	-	-	5	-	-	10
	Q1 ①	V_{OL}	9	-	0.4	Vdc	-	0.4	Vdc	9	-	-	-	-	-	2,3	6,7	1	-	5	-	-	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	2,3,6,7	1	-	-	5	1	9,10
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	9	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
	Q2 ①	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	↓	-	-	-	5	1	8,10
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	-	↓	1	-	5	-	-	10
	Q3 ①	V_{OL}	11	-	0.4	Vdc	-	0.4	Vdc	11	-	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	6,7	2,3	↓	-	-	5	-	10,11
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	11	-	-	-	-	6,7	2,3	↓	-	5	-	-	10
Power Requirements (Total Device)																						
Power Supply Drain		I_{PD}	5	-	46	mAdc	-	53	mAdc	-	-	-	-	-	-	-	-	-	-	-	5	-	6,7,10

Pulse 1: Apply positive pulse prior to taking measurement to set the device in the desired state. $V_{th\,H}$ (2.2 V) Maintain $V_{th\,L}$ voltage for measurement. $V_{th\,L}$

① All input, power supply and ground voltages must be maintained between each test unless otherwise noted.

SWITCHING TIME TEST CIRCUIT



f_{Tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

VOLTAGE WAVEFORMS AND DEFINITIONS