MOTOROLA

Microprocessor and Memory Technologies Group

MC68340

UPDATE TO
MC68340 Integrated Processor With DMA User's Manual and Addendum

November 3, 1995

CORRECTIONS TO "MC68340 INTEGRATED PROCESSOR WITH DMA USER'S MANUAL"

1. Negation of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ for Retry Sequence and Late Retry Sequence.

Figure 3-19 and Figure 3-20 on pages 3-37 and 3-38 respectively, should show $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ being negated one-half clock cycle earlier. Figure 1 and Figure 2 in this document show the corrected diagrams.

2. Typo in Channel Status Register (CSR) description.

The last sentence for the IRQ bit description on page 6-31 should be changed to "The STR bit in the CCR cannot be set when this bit is set; all error status bits must be cleared before the STR bit can be set."

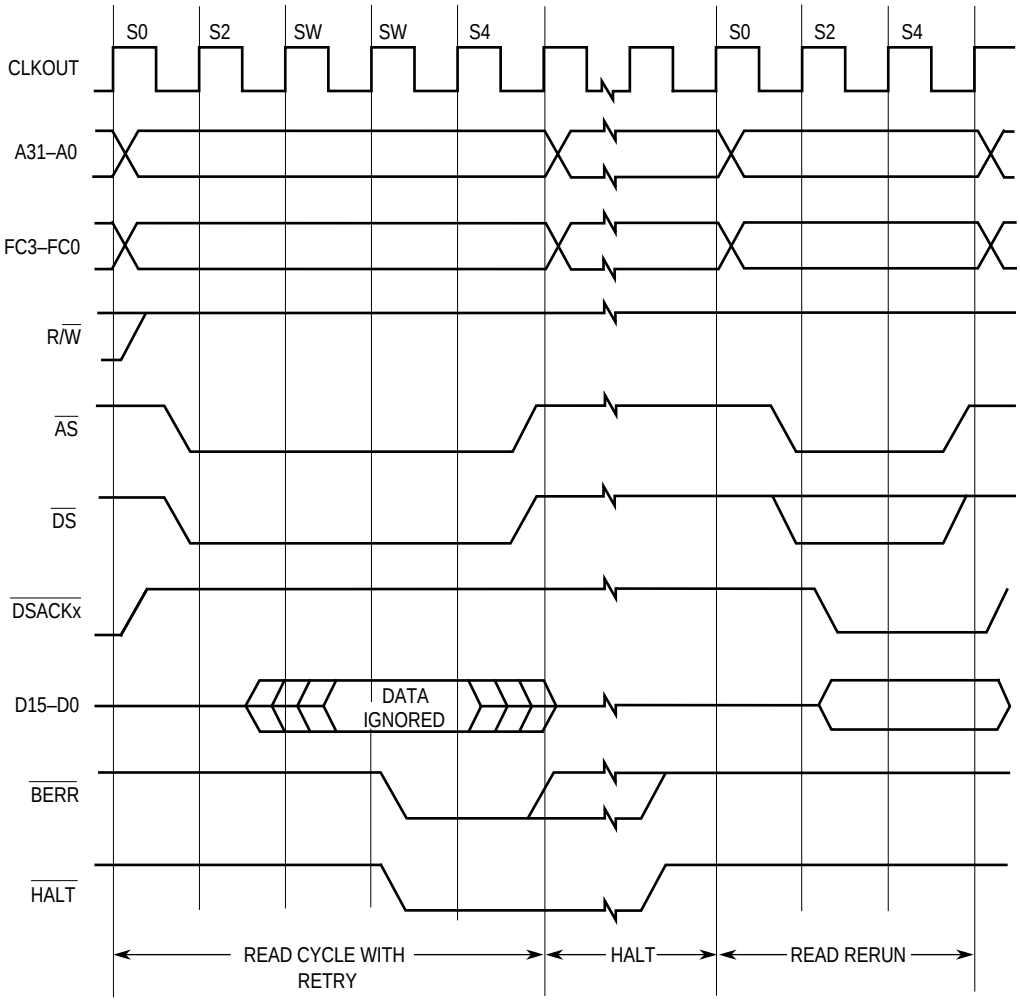


Figure 1. Retry Sequence

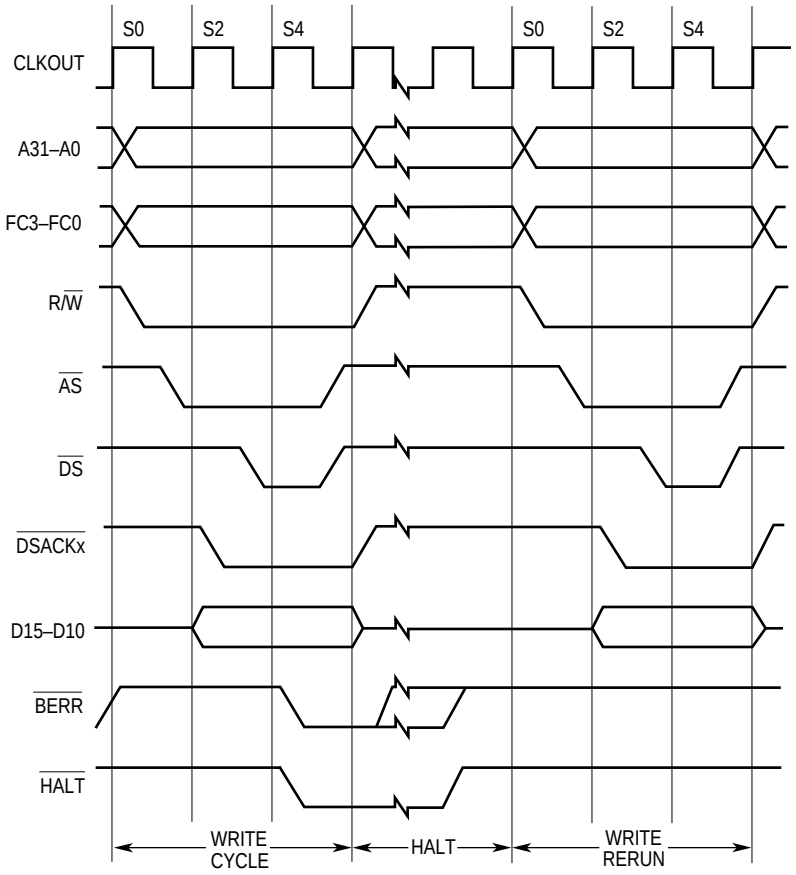


Figure 2. Late Retry Sequence

CORRECTIONS TO “ADDENDUM TO MC68340 INTEGRATED PROCESSOR WITH DMA USER’S MANUAL - REV 1”

3. Standard MC68340 Ordering Information

The table in item 70 on page 17 of the “MC68340 User’s Manual Addendum” incorrectly labels the frequency of the MC68340PV25 as 0-8.39MHz. The actual frequency is 0-25MHz. The information is corrected in Table 1 of this document.

Table 1. Standard MC68340 Ordering Information

Supply Voltage	Package Type	Frequency (MHz)	Temperature	Order Number
5.0 V	Ceramic Quad Flat Pack FE Suffix	0 – 16.78 0 – 16.78 0 – 25	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340FE16 MC68340CFE16 MC68340FE25
5.0 V	Plastic Pin Grid Array RP Suffix	0 – 16.78 0 – 16.78 0 – 25	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340RP16 MC68340CRP16 MC68340RP25
5.0 V	Thin Quad Flat Pack PV Suffix	0 – 16.78 0 – 25	0° C to 70° C 0° C to 70° C	MC68340PV16 MC68340PV25
3.3 V	Thin Quad Flat Pack PV Suffix	0 – 16.78 0 – 8.39	0° C to 70° C 0° C to 70° C	MC68340PV16V MC68340PV8V
3.3 V	Ceramic Quad Flat Pack FE Suffix	0 – 8.39 0 – 8.39 0 – 16.78	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340FE8V MC68340CFE8V MC68340FE16V
3.3 V	Plastic Pin Grid Array RP Suffix	0 – 8.39 0 – 8.39 0 – 16.78	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340RP8V MC68340CRP8V MC68340RP16V

4. Typo on PV pin assignment diagram

The pin assignment diagram for the PV package on page 18 of the “MC68340 User’s Manual Addendum” is incorrect. Pin numbers 75, 80, and 85 should be moved up one pin. The corrected diagram is shown in Figure 3.

5. Missing dimension in PV case outline drawing.

The case outline drawing of the PV package on page 19 of the “MC68340 User’s Manual Addendum” is missing the J dimension. The corrected case outline drawing is shown in Figure 4.

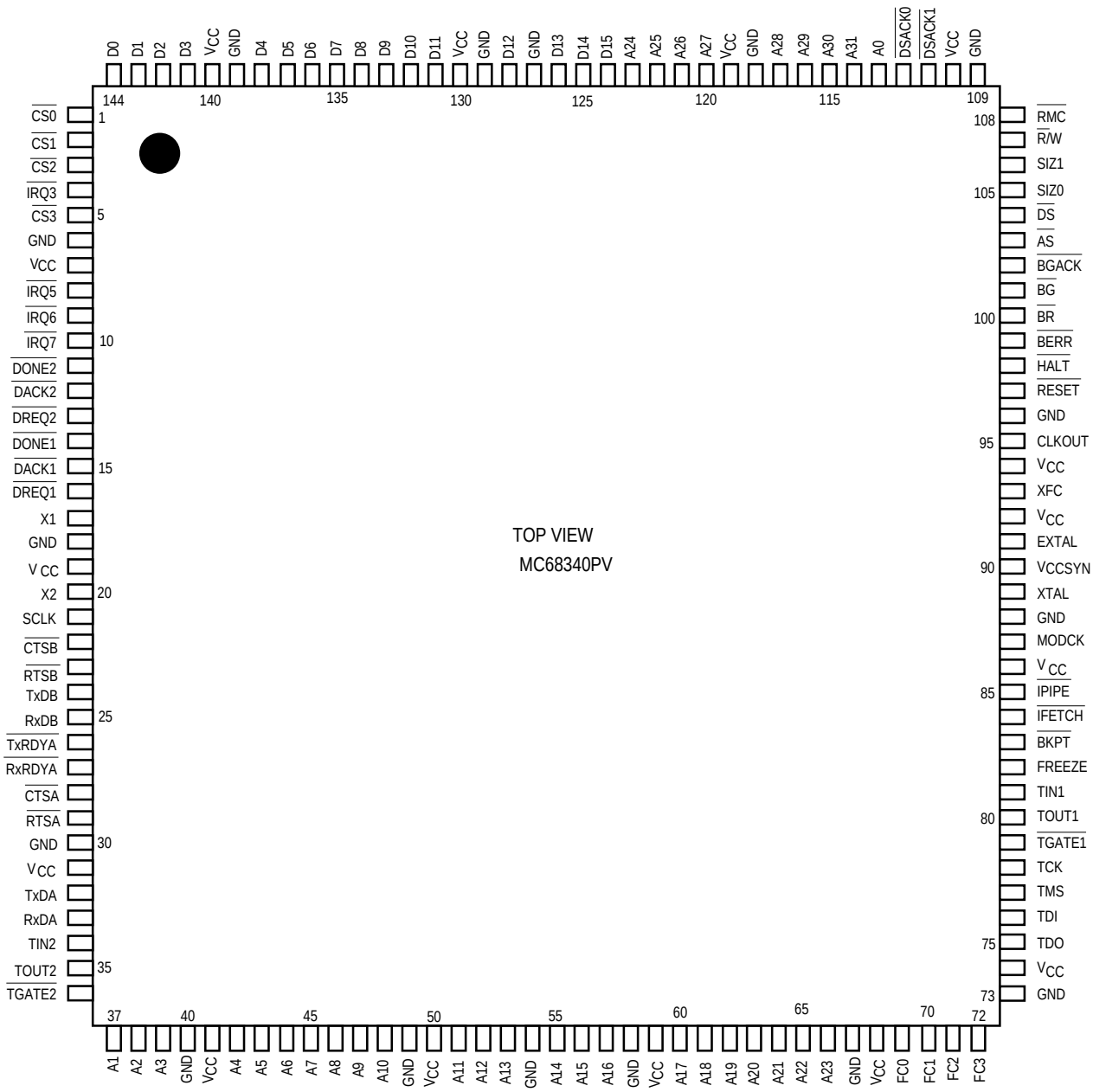
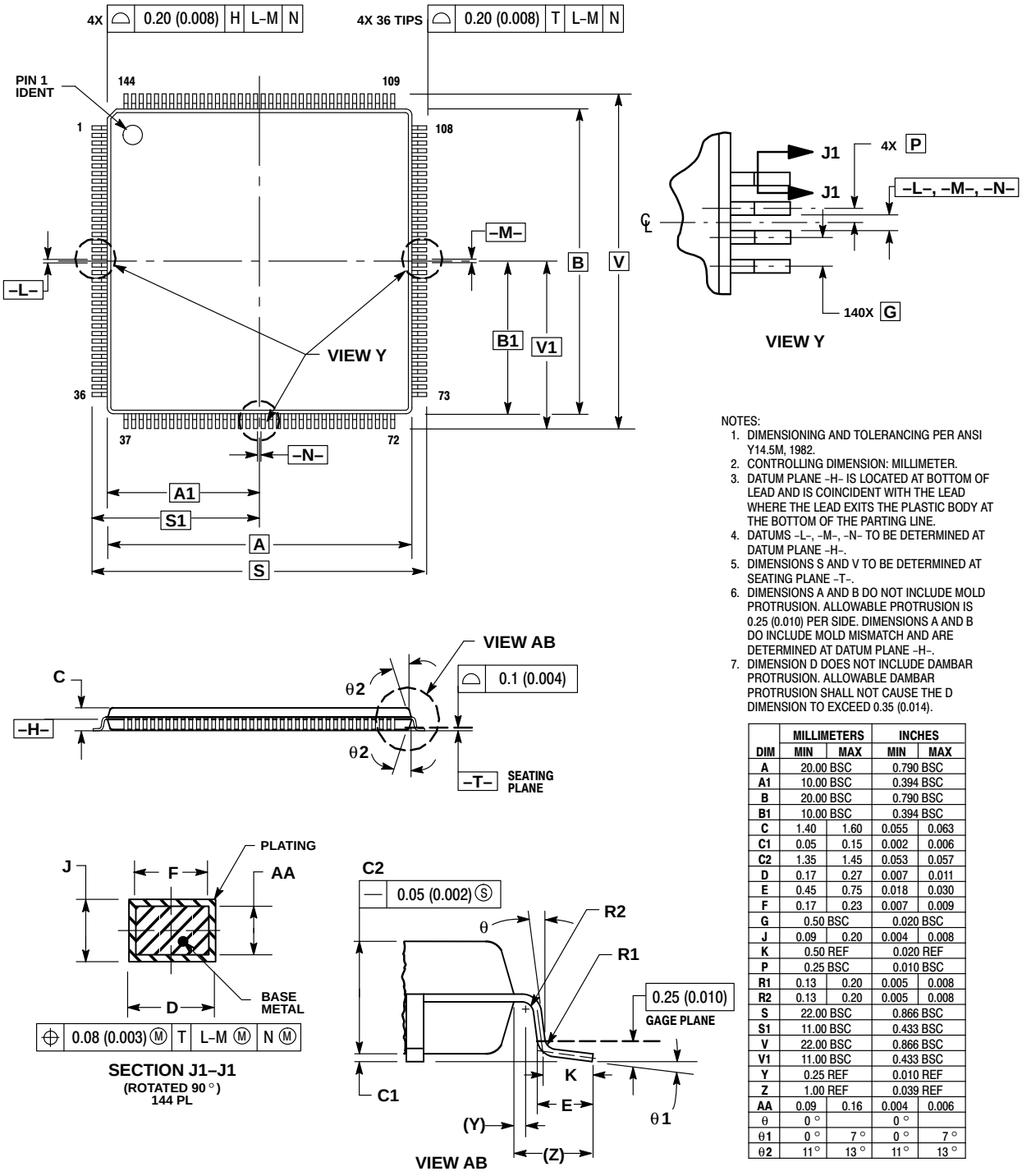


Figure 3. 144-Lead Thin QUAD Flat Pack (PV Suffix)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M-, -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35 (0.014).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.00 BSC		0.790 BSC	
A1	10.00 BSC		0.394 BSC	
B	20.00 BSC		0.790 BSC	
B1	10.00 BSC		0.394 BSC	
C	1.40	1.60	0.055	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.17	0.27	0.007	0.011
E	0.45	0.75	0.018	0.030
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
P	0.25 BSC		0.010 BSC	
R1	0.13	0.20	0.005	0.008
R2	0.13	0.20	0.005	0.008
S	22.00 BSC		0.866 BSC	
S1	11.00 BSC		0.433 BSC	
V	22.00 BSC		0.866 BSC	
V1	11.00 BSC		0.433 BSC	
Y	0.25 REF		0.010 REF	
Z	1.00 REF		0.039 REF	
AA	0.09	0.16	0.004	0.006
θ	0 °		0 °	
θ1	0 °	7 °	0 °	7 °
θ2	11 °	13 °	11 °	13 °

Figure 4. Package Dimensions (PV suffix)

UPDATES TO “MC68340 INTEGRATED PROCESSOR WITH DMA USER’S MANUAL”

6. Plastic QFP package (FT suffix) pinout and case outline.

The plastic QFP package (FT suffix) pinout is the same as the CQFP package (FE suffix). The pinout and mechanical information for the plastic QFP package are shown in Figure 5 and Figure 6.

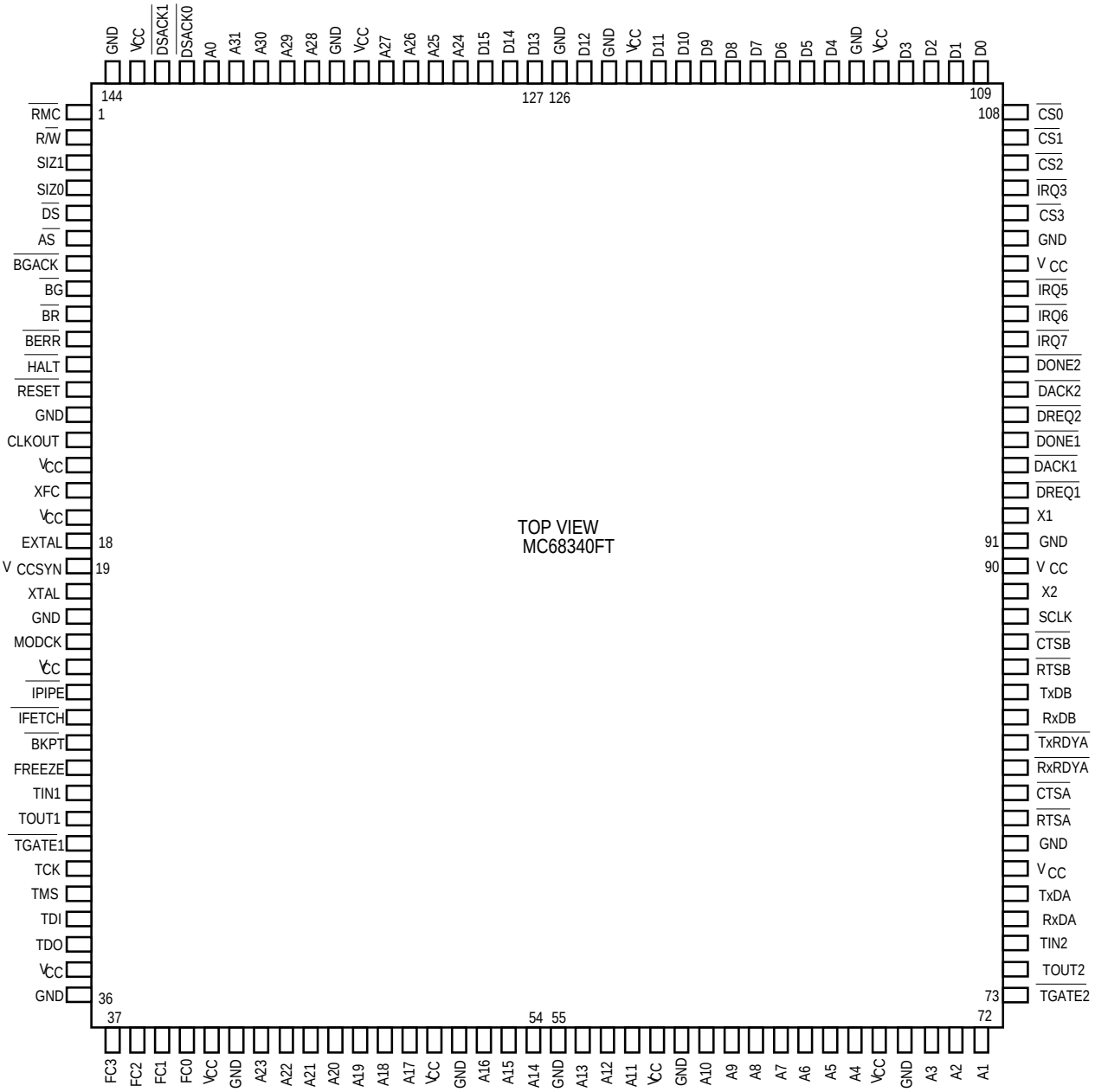
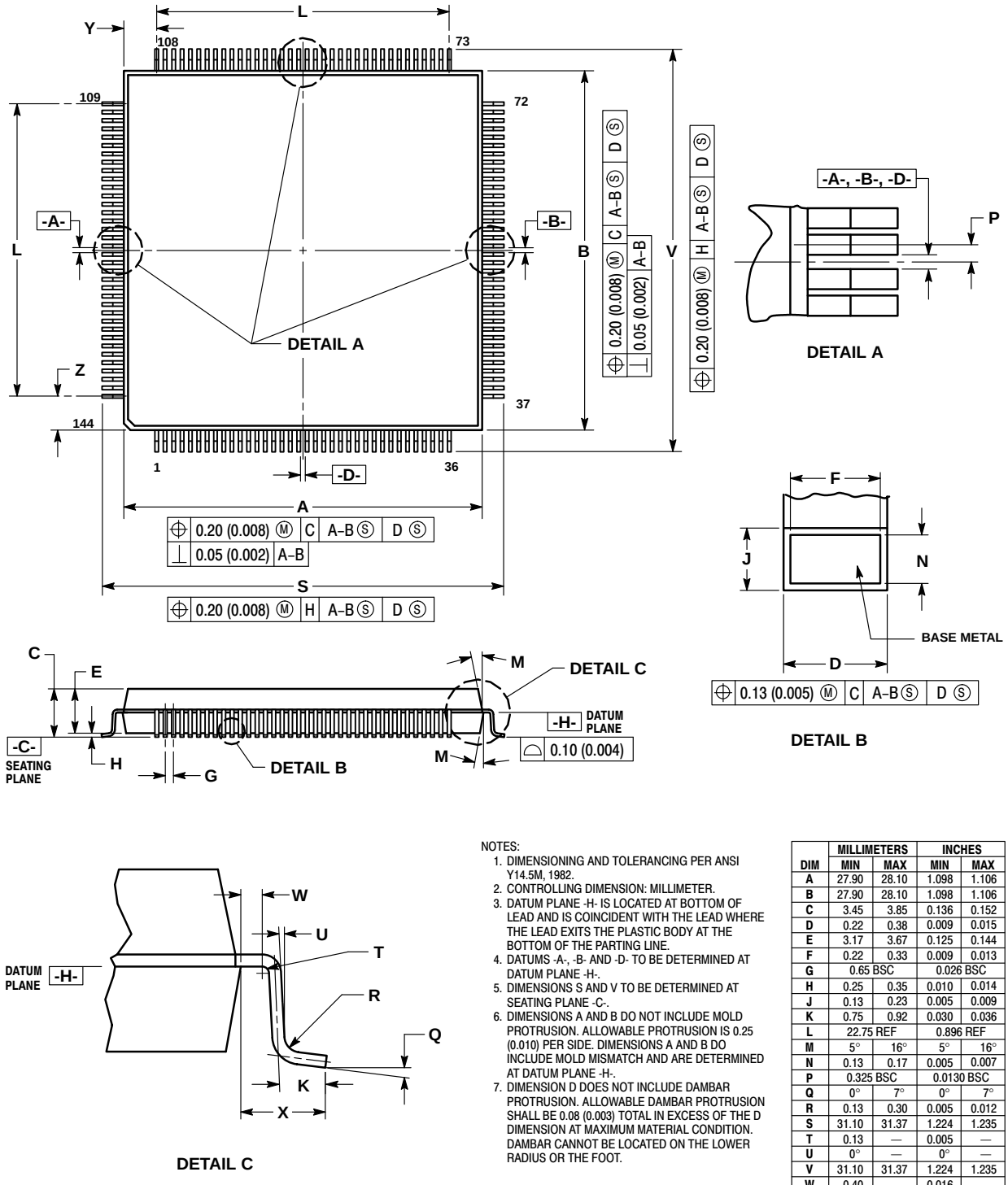


Figure 5. 144-Lead Plastic Quad Flat Pack (FT suffix)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	3.85	0.136	0.152
D	0.22	0.38	0.009	0.015
E	3.17	3.67	0.125	0.144
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	0.25	0.35	0.010	0.014
J	0.13	0.23	0.005	0.009
K	0.75	0.92	0.030	0.036
L	22.75 REF		0.896 REF	
M	5°	16°	5°	16°
N	0.13	0.17	0.005	0.007
P	0.325 BSC		0.0130 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.10	31.37	1.224	1.235
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.10	31.37	1.224	1.235
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	2.63 REF		0.104 REF	
Z	2.63 REF		0.104 REF	

Figure 6. Package Dimensions (FT suffix)

7. Additional information on PV package pin groupings.

The VCC and GND pins are separated into groups to help electrically isolate the output drivers for different functions of the MC68340. These groups are shown in Table 2 for the PV suffix package.

Table 2. Pin Groups (PV Suffix)

Pin Group — PV Suffix	VCC	GND
Address Bus, Function Codes	41, 50, 59, 68, 119	40, 49, 58, 67, 118
Data Bus	130, 140	129, 139
$\overline{AS}$, $\overline{BG}$, $\overline{CLKOUT}$, $\overline{DS}$, $\overline{FREEZE}$, $\overline{HALT}$, $\overline{IFETCH}$, $\overline{IPIPE}$, MODCK, $\overline{RESET}$, $\overline{RMC}$, R/$\overline{W}$, SIZx, TDO, TOUT1, Internal Logic	74, 92, 94, 110	73, 88, 96, 109
$\overline{CSx}$, $\overline{DACKx}$, $\overline{DONEx}$, $\overline{IRQx}$, $\overline{RTSx}$, $\overline{RxRDYA}$, TOUT2, TxDx, $\overline{TxRDYA}$, Internal Logic	7, 19, 31	6, 18, 30
Oscillator	90	—
Internal Only	86	54, 127

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