M MOTOROLA

MC68HC09E

Product Preview

8-BIT HCMOS MICROPROCESSING UNIT

The MC68HC09E is a revolutionary low-power high-performance 8-bit HCMOS microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC68HC09E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC68HC09E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems, or other MPUs.

HARDWARE FEATURES
- Very Low-Power High-Density CMOS
- External Clock Inputs, E and Q, Allow Synchronization
- TSC Input Controls Internal Bus Buffers
- LIC Indicates Opcode Fetch
- AVMA Allows Efficient Use of Common Resources in a Multiprocessor System
- BUSY is a Status Line for Multiprocessing
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- Interrupt Acknowledge Output Allows Vectoring by Devices
- Sync Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle $\overline{RESET}$
- Single 5-Volt Supply Operation
- $\overline{NMI}$ Inhibited After $\overline{RESET}$ Until After First Load of Stack Pointer
- Early Address Valid Allows Use with Slower Memories
- Early Write Data for Dynamic Memories

SOFTWARE FEATURES
- 10 Addressing Modes
  - M6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing
    - 0-, 5-, 8-, or 16-Bit Constant Offsets
    - 8- or 16-Bit Accumulator Offsets
    - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instruction with Unique Addressing Modes
- 8 × 8 Unsigned Multiply
- 16-Bit Arithmetic
- Transfer/Exchange All Registers
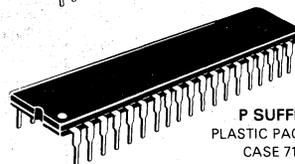- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

HCMOS
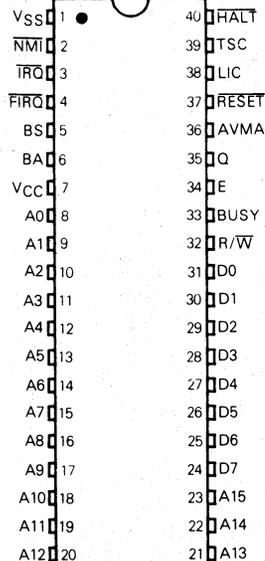(HIGH-DENSITY CMOS SILICON-GATE)

8-BIT HCMOS MICROPROCESSING UNIT
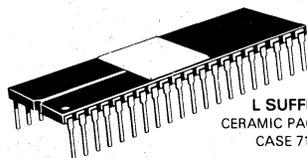
L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT

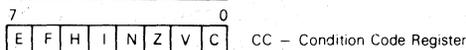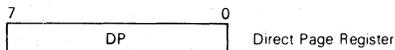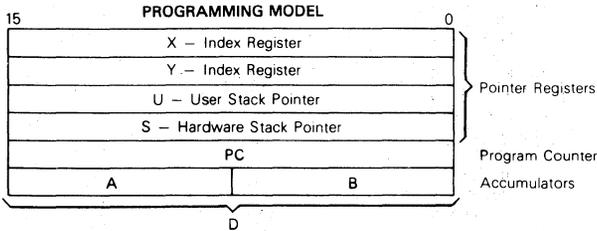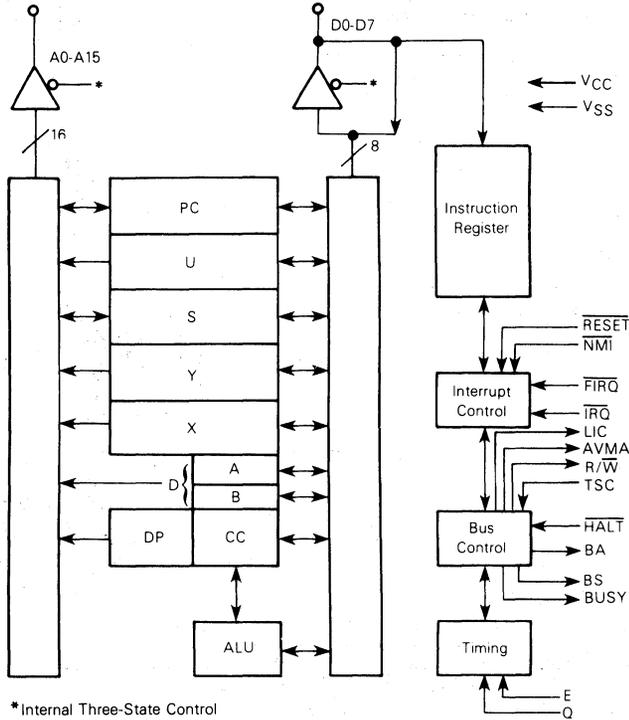|			
V$_{SS}$	1 ●	40	$\overline{HALT}$
$\overline{NMI}$	2	39	TSC
$\overline{IRQ}$	3	38	LIC
$\overline{FIRQ}$	4	37	$\overline{RESET}$
BS	5	36	AVMA
BA	6	35	Q
V$_{CC}$	7	34	E
A0	8	33	BUSY
A1	9	32	R/$\overline{W}$
A2	10	31	D0
A3	11	30	D1
A4	12	29	D2
A5	13	28	D3
A6	14	27	D4
A7	15	26	D5
A8	16	25	D6
A9	17	24	D7
A10	18	23	A15
A11	19	22	A14
A12	20	21	A13

MC68HC09E

ARCHITECTURAL FEATURES
- Two 16-Bit Index Registers
- Two 16-Bit Indexable Stack Pointers
- Two 8-Bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

MC6800 COMPATIBLE
- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

EXPANDED BLOCK DIAGRAM

*Internal Three-State Control

PROGRAMMING MODEL

15   0

| X — Index Register |
| Y — Index Register |
| U — User Stack Pointer |
| S — Hardware Stack Pointer |

Pointer Registers

| PC |

Program Counter

| A | B |

Accumulators

D

7   0

| DP |

Direct Page Register

7   0

| E | F | H | I | N | Z | V | C |

CC — Condition Code Register

CONDITION CODE REGISTER FORMAT

| E | F | H | I | N | Z | V | C |

- Carry
- Overflow
- Zero
- Negative
- IRQ Mask
- Half Carry
- FIRQ Mask
- Entire Flag