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MC68PM302

Product Brief

Integrated Multiprotocol Processor with PCMCIA

Motorola introduces a version of the well-known MC68302 Integrated Multiprotocol Processor (IMP) with an integrated PCMCIA controller. It is known as the MC68PM302, and expands a family of devices based on the MC68302.

The MC68PM302 incorporates some enhancements over the standard MC68302 like a static core, a periodic interrupt timer and low power modes.

The MC68PM302 has two modes of operation. In the first mode, the MC68PM302 offers additional parallel I/O pins compared to the standard MC68302. In the second mode of operation the parallel I/O takes the functionality of the PCMCIA and 16550 UART interfaces.

The MC68PM302 is packed in a low profile 144 TQFP package that is suitable for use in Type II PCMCIA cards.

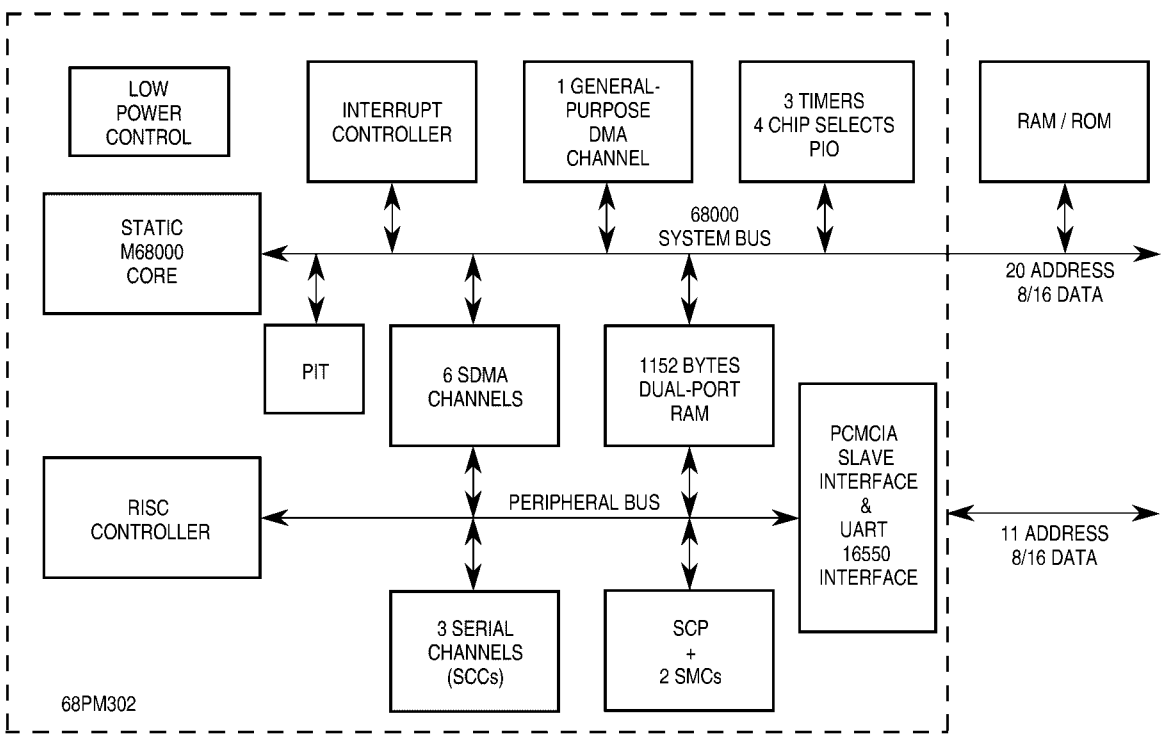

Figure 1. MC68PM302 Block Diagram

SEMICONDUCTOR PRODUCT INFORMATION

The Personal Computer Memory Card International Association (PCMCIA) has implemented a set of specifications for small form-factor cards. These cards were previously specified by a version number of the spec to which they complied. After specification 2.1, these cards were named "PC Cards." The PCMCIA functionality on the MC68PM302 complies with the specification approved in October 1994.

In addition, the MC68PM302 contains a parallel interface and register set identical to the 16550 UART used in IBM-compatible PCs. This functionality is available when the PCMCIA mode is enabled, and shares pins with the PCMCIA interface.

FEATURES

The features of the MC68PM302 are as follows. The items in **bold face** type show major differences from the MC68302.

- On-Chip **Static 68000 Core** Supporting a 16- or 8-Bit M68000 Family-System
- SIB Including:
  - — Independent Direct Memory Access (IDMA) Controller.
  - — Interrupt Controller with Two Modes of Operation
  - — Parallel Input/Output (I/O) Ports, Some with Interrupt Capability
  - — On-Chip 1152-Byte Dual-Port RAM
  - — Three Timers Including a Watchdog Timer
  - **— New Periodic Interrupt Timer (PIT)**
  - — Four Programmable Chip-Select Lines with Wait-State Generator Logic
  - — Programmable Address Mapping of the Dual-Port RAM and IMP Registers
  - — On-Chip Clock Generator with Output Signal
  - — Glueless Interface to EPROM, SRAM, Flash EPROM, and EEPROM
  - — Allows Boot in 8-Bit Mode, and Running Switch to 16-Bit Mode
  - — Allows System Clock to be Generated from 32 kHz or 4 MHz crystals in Addition to a Full Speed Clock Oscillator
  - — System Control:
    - System Status and Control Logic
    - Disable CPU Logic (Slave Mode Operation)
    - Hardware Watchdog
    - New Low-Power (Standby) Modes in µA Range With Wake-up from Two Pins or PIT Timer
    - Freeze Control for Debugging
    - DRAM Refresh Controller
  - — CP Including:
  - — Main Controller (RISC Processor)
  - — Three Independent Full-Duplex Serial Communications Controllers (SCCs)
  - — Supporting Various Protocols:
    - High-Level/Synchronous Data Link Control (HDLC/SDLC)
    - Universal Asynchronous Receiver Transmitter (UART)
    - Binary Synchronous Communication (BISYNC)
    - Transparent Modes
    - Autobaud Support Instead of DDCMP
    - V.110 Rate Adaption
  - — Six Serial DMA Channels for the Three SCCs
  - — Flexible Physical Interface Accessible by SCCs Including ISDN Support:

Motorola Interchip Digital Link (IDL)
General Circuit Interface (GCI, also known as IOM-2[1])
Pulse Code Modulation (PCM) Highway Interface
Nonmultiplexed Serial Interface (NMSI) Implementing Standard
Modem Signals

— SCP for Synchronous Communication

— Two Serial Management Controllers (SMCs) To Support IDL and GCI Auxiliary Channels

- **PCMCIA Controller**
  - **— Supports Slave Interface Having 8 or 16-bit Data Pins**
  - **— Compatible with the PC Card Classic Specification Approved in October 1994**
  - **— Support for Ring Detect and Other Indications**
  - **— Support for Power Down Modes and Automatic Wakeup on Host Access**
  - **— Card Information Structure (CIS) Size and Location In Memory Programmable**
  - **— Supports DMA Accesses as Defined by PCMCIA**
  - **— Supports DMA Direct Access to Common Memory Space for High Speed Buffer Transfers**
  - **— Security Option to Prevent Host Accesses to Sensitive Address Ranges**
  - **— Separate PCMCIA Reset Signal**
- **16550 Emulation Block**
  - **— Complete H/W and S/W Emulation of the 16550 UART**
  - **— DMA Supported for Transfer of 16550 Data Over 68K Bus**
  - **— Speed of Data Transfer Can Be Matched to Traditional 16550 UART**
  - — High Speed Data Transfer up to 2 Mbps Possible
- Initial Offering Features 16.67 and 20 MHz Versions at 5V and 3.3V
- 144 Pin Thin Quad Flat Pack (TQFP) Packaging

MC68PM302 APPLICATIONS

The MC68PM302 excels in several applications areas.

First, the MC68PM302 excels in low power and portable applications. The inclusion of a static 68000 core, coupled with the low power modes built into the device, make it ideal for handheld or other low power applications. The new 32 kHz or 4 MHz PLL option greatly reduces the total power budget of the designer's board, and allows the MC68PM302 to be an effective device in low power systems. The MC68PM302 can then optionally generate a full frequency clock for use by the rest of the board. During low power modes, the new periodic interrupt timer (PIT) allows the device to awaken at regular intervals. In addition, two pins can awaken the device from low power modes. These features make the device useful as an upgrade to the existing MC68302.

Second, the performance, cost, and low powerconsumption of the MC68PM302 makes it an ideal processor for PCMCIA cards. It will perform the controller functions of a V.34 fax/data modem in conjunction with a separate data pump. With its PCMCIA and ISDN functionality on-chip, it can be gluelessly connected to an S/T or U interface device to perform the functions of a ISDN terminal adaptor. It can be used as a MAC

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1. IOM is a trademark of Siemens AG

controller for IEEE 802.11 wireless LANs. It may also be used as a wireless WAN PCMCIA controller for CDPD, Ardis, Mobitex, or digital cellular data applications.

DIFFERENCES BETWEEN THE MC68PM302 AND OTHER 302 FAMILY DEVICES

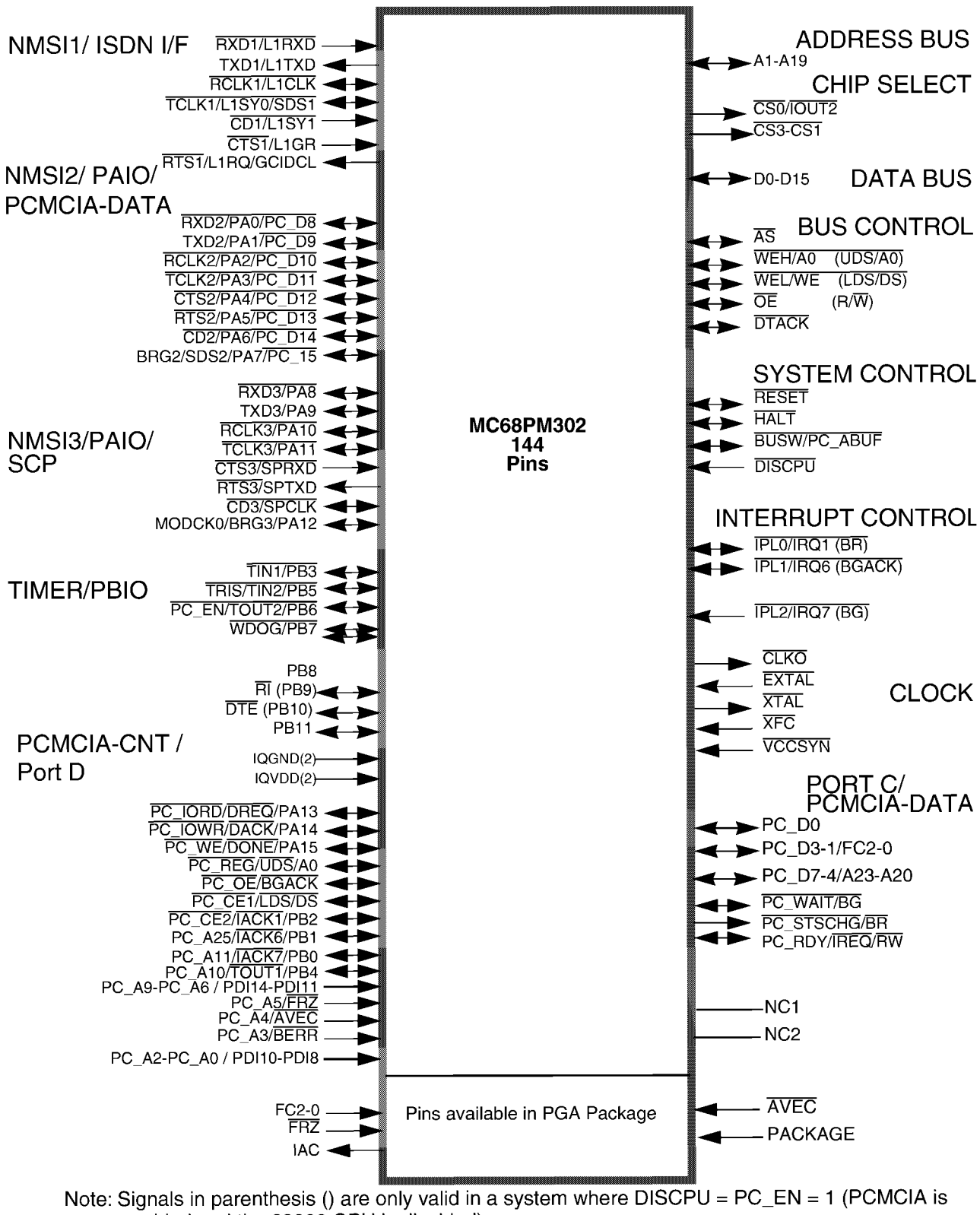
The MC68PM302 can be considered as a superset of another derivative called the MC68LC302. The MC68LC302 does not have the PCMCIA and 16550 features, and only contains 2 SCCs. The MC68PM302 can also be considered to be a subset of the MC68356. The 356 adds a full 56002 DSP with memory and, in one of its versions, contains a full V.34 fax/data data pump running on the DSP.

When the MC68PM302 is operating in its PCMCIA mode, certain functions existing on the original MC68302 are no longer available. The major differences are listed below.

- External masters are not able to take the bus away from the MC68PM302 through the normal bus arbitration scheme as these pins no longer exist. An external master can still maintain bus mastership through a simple scheme using the $\overline{\text{HALT}}$ pin. This restriction does not apply when using the MC68PM302 in CPU disabled mode (slave mode), in which case $\overline{\text{BR}}$, $\overline{\text{BG}}$, and $\overline{\text{BGACK}}$ are all available.
- Although the Independent DMA (IDMA) is still available, the external IDMA request pins ($\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$) have been eliminated. IDMA transfers can only originate under CPU control.
- Four address lines have been eliminated, giving a total of 20 address lines. However, the MC68PM302 supports more than a 1 MB addressing range, since each of the four chip selects still decodes a 24-bit address. This allows a total of 4 MB to be addressed.
- The $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, and R/$\overline{\text{W}}$ pins are not available except in slave mode, where they replace the $\overline{\text{IPL2-0}}$ pins. Instead, the new pins $\overline{\text{WEH}}$, $\overline{\text{WEL}}$, and $\overline{\text{OE}}$ have been defined for glueless interfacing to memory.
- PA12 is now muxed with the MODCLK pin, which is associated with the 32 KHz or 4 MHz PLL. The MODCLK pin is sampled at reset, and then becomes the PA12 pin.
- New VCCsyn, GNDsyn, and XFC pins have been added in support of the on-chip PLL.
- For purposes of emulation and development support only, a special 180 PGA version is supported. This version adds back the FC2-0, $\overline{\text{IAC}}$, $\overline{\text{FRZ}}$, and $\overline{\text{AVEC}}$ signals to non multiplexed pins. In the TQFP package when operating in PCMCIA mode, these signals are not available. The FC2-0 pins allow bus cycles to be distinguished between program and data accesses, interrupt cycles, etc. The $\overline{\text{IAC}}$, $\overline{\text{FRZ}}$, and $\overline{\text{AVEC}}$ pins are provided so that emulation vendors can quickly retrofit their existing MC68302 emulator designs to support the MC68PM302.

When the MC68PM302 is not used in its PCMCIA mode, most of the original MC68302 pins are returned to the device. However, even though the MC68302 is also offered in a 144 TQFP, it was not possible to make the MC68PM302 exactly pin compatible with the original MC68302. Thus, the MC68PM302 should not be used as a drop-in replacement for the MC68302 in a 144 TQFP.

MC68PM302 PIN DESCRIPTION



Note: Signals in parenthesis () are only valid in a system where DISCPU = PC_EN = 1 (PCMCIA is enabled and the 68000 CPU is disabled).

Table 1. MC68PM302 Ordering Information

Package Type	Operating Voltage	Frequency (MHz)	Temperature	Order Number
Pin Grid Array (RC Suffix)	5V	20	0°C to 70°C	MC68PM302RC20
Thin Quad Flat Pack (PVSuffix)	5V 5V 5V 5V	16.67 16.67 20 20	0°C to 70°C –40°C to +85°C 0°C to 70°C –40°C to +85°C	MC68PM302PV16 TBD TBD TBD
Thin Quad Flat Pack (PV suffix)	3.3V 3.3V 3.3V 3.3V	16.67 16.67 20 20	0°C to 70°C –40°C to +85°C 0°C to 70°C –40°C to +85°C	MC68PM302PV16V TBD TBD TBD

Table 2. Documentation

Document Title	Order Number	Contents
MC68302 User's Manual	MC68302UM/AD	Detailed information for design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
The 68K Source	BR729/D	Independent vendor listing supporting software and development tools
The MC68PM302 Addendum		Describes the differences between the MC68302 and the MC68PM302

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION