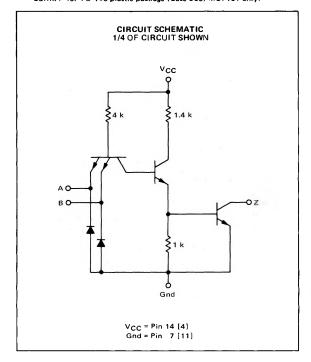
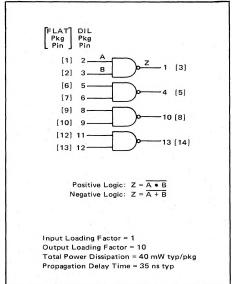
QUAD 2-INPUT "NAND" GATE WITH OPEN COLLECTOR

MC5401 · MC7401

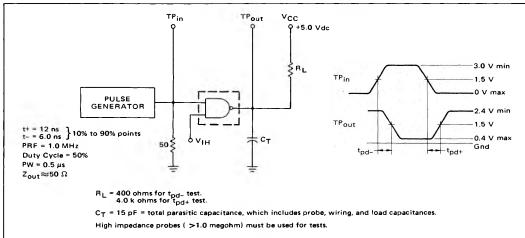
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7401 only.



This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC5401, MC7401 (continued)

				[1] 2_	4 8	N	1	[3]													
>	V = VCC = Pin 14 [4] Gnd = Pin 7 [11]	VCC = Pin 14 [4] Gnd = Pin 7 [11]					—4 [5] —10 [8]	<u> </u>													
ELECTRICAL CHARACTERISTICS	RACTE	RISTIC		12] 11— 13] 12—			—13 [14]	4													
Test procedures are shown for only one	own for	only on	ē						81,		F	EST CUR	RENT/VO	TEST CURRENT/VOLTAGE VALUES		(All Temperatures)	tures)				
gate. The other gates are tested in the same	tested in	the sam	91						μA					Volts	lts						
manner. Further, test procedures are shown for only one input of the gate under test.	ocedures;	are show nder tes	نه ع						lor	VIL	V _H	\ ННІ А	V _{R1}	V _{R2}	V _{th 1}	V _{th} 0	V _{CEX}	Vcc	V _{CCL}	V _{ссн}	
To complete testing, sequence through remaining inputs.	quence th	rough r	ф				M M	MC5401	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.50	5.50	Pin 7[11] is grounded
		Pin		MC5401 Test Limits -55 to +125°C	Limits 25°C	MC740	MC7401 Test Limits 0 to +70°C	mits			1 -	STCURF	SENT/VOL	TAGE APF	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:	NS LISTE	D BELO	N:			for all tests in addi- tion to the pins listed below:
Characteristic	Symbol	Test	-	Мах	Tim	Min	Max	ij	_6	\ 	> H	> HH	V _{R1}	V _{R2}	V _{th 1}	V	VCEX	رد ۷	Vccı	V _{ссн}	Gnd
Input Forward Current	I,	A		-1.6	mAdc	100	-1.6	mAdc		4			В		1	1	ī	1		>	*
Leakage Current	IRI	A	1	40	μAdc		40	μAdc			A		1	ľ	1			1	1	>	B *
	$^{\rm L}_{ m R2}$	Ą		1.0	mAdc	1	1.0	mAdc	T		-1	A				4				>	B *
Output Output Voltage	NOL	Z		0.4	Vdc		0.4	Vdc	И		7				A,B	1		1	>	1	*
Output Leakage Current	ICEX	Z		0.25	mAdc	1	0.25	mAdc	1		1		4	111		В	Z	1	Λ	1	*
Power Requirements (Total Device) Power Supply Drain	ндал	۸		22	mAdc		22	mAdc					L.	All Inputs	51 - 7	t .	r	- 7.1.7	L T -	Λ	
	$I_{\rm PDL}$	۸		8.0	mAdc		8.0	mAdc		1	1	1	, i.,		i,			1	ï	Λ	A,B*
Switching Parameters									Pulse	Pulse Out											
Turn-On Delay	t pd-	A,Z	, L	15**	ns		15**	su	4	Z	В	1		ī		7	. 1	>	1	L	ı
Turn-Off Delay	tpd+	A,Z		42**	su	Į.	42**	su	A.	z	В		r	3 3 1 2 1	1	1	i.	>	1	1	1
							1	1	-		1	1									

*Ground inputs to gates not under test.
**Tested only at 25°C.