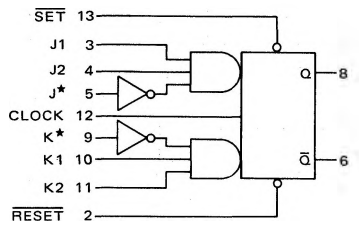
J-K FLIP-FLOP

MC5470L*
MC7470L,P*



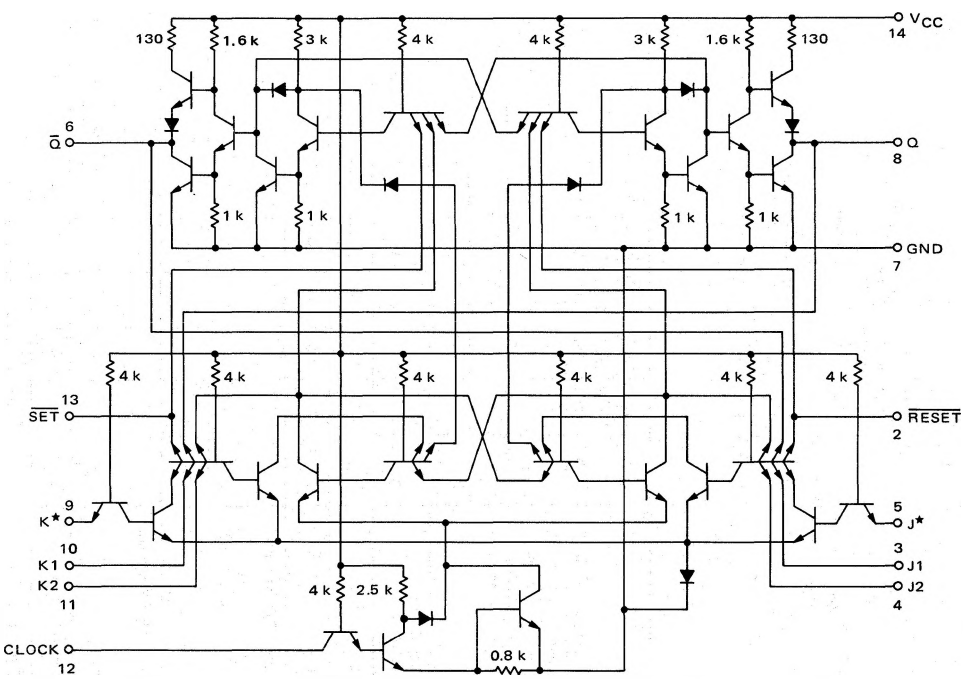
This J-K flip-flop triggers on the positive edge of the clock pulse. The multiple-input gating configuration helps minimize package count in J-K flip-flop applications requiring AND gating at the inputs. This device requires relatively fast clock rise and fall times (≤ 150 ns) but is more suitable for use in high-speed systems since information may be applied to, or changed at the steering inputs any time in a clock cycle except during the interval of time between the setup and hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section when the clock goes low. The input steering section continually reflects the input states when the clock is low. The flip-flop can be set or reset directly by applying a logic "0" to $\overline{SET}$ or $\overline{RESET}$, respectively, while clock is at logical zero level

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$J = J1 \cdot J2 \cdot \overline{J^*}$
$K = K1 \cdot K1 \cdot \overline{K^*}$

Output Loading Factor = 10
Total Power Dissipation = 65 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 35 MHz typ

* L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.



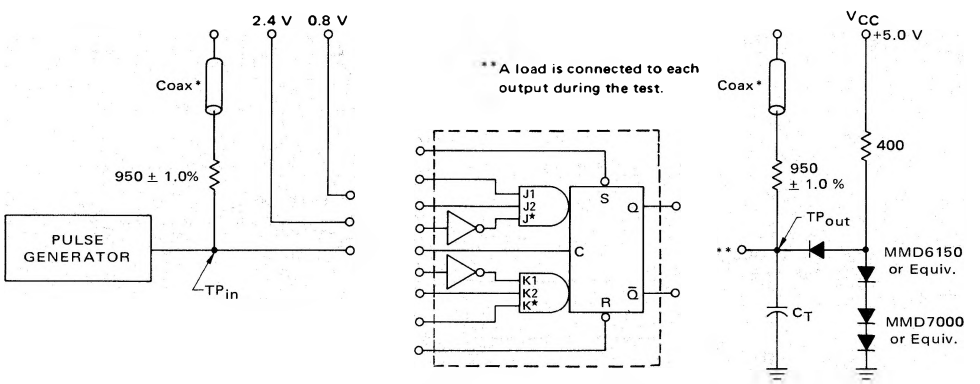
OPERATING CHARACTERISTICS

Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock pulse. Steering data should be present 20 ns prior to rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs should be applied only when clock is low. A low input to $\overline{SET}$ sets Q to a logic "1"; a low input to $\overline{RESET}$ sets $\bar{Q}$ to a logic "1".

Unused inputs: If J* and K* are not used they should be grounded. Unused $\overline{SET}$ and $\overline{RESET}$ inputs should be tied to a voltage between 2.4 and 5.5 Vdc.
Unused J or K inputs should be tied to the used J or K inputs, respectively, or to a voltage between 2.4 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and CLOCK tests.

* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

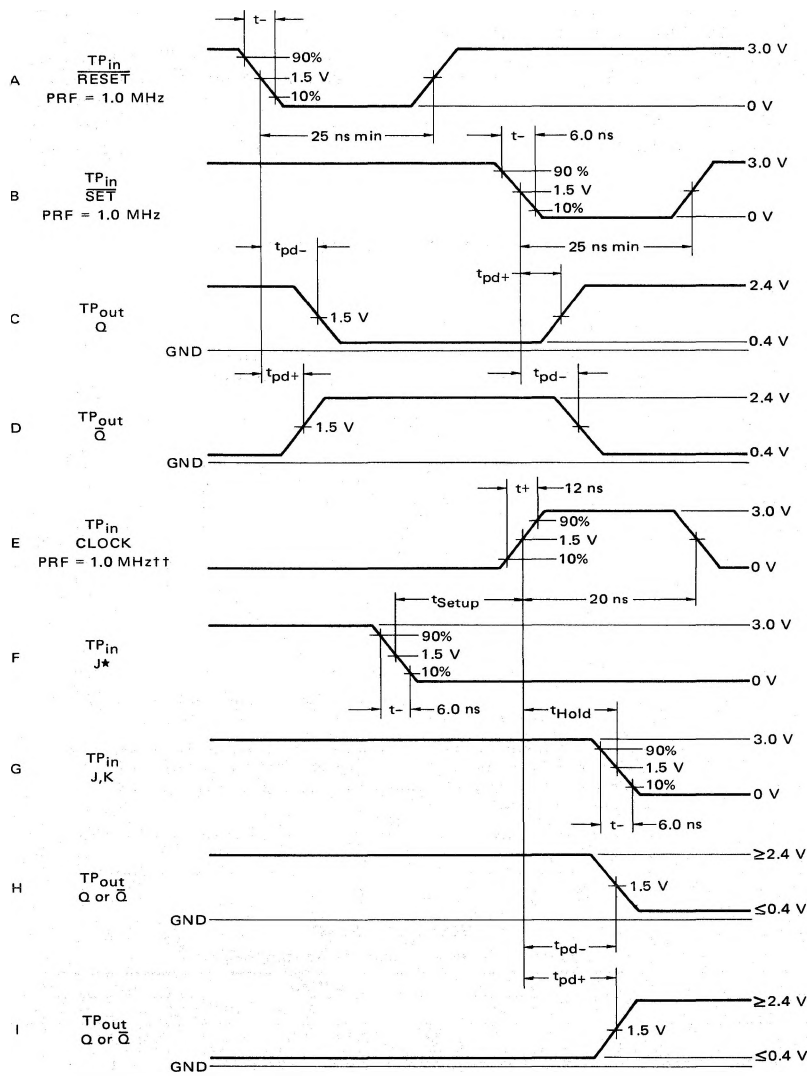
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT							Q	$\bar{Q}$	LIMITS		
		C	J	K	J*	K*	$\bar{R}$	$\bar{S}$			Min	Max	Unit
Toggle Frequency	t_{Tog}	E	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	†	†	20	–	MHz
Turn-On Delay from $\overline{SET}$ or $\overline{RESET}$	t_{pd-}*	0.8 V	5.0 V	5.0 V	Gnd	Gnd	A	B	C	D	–	50	ns
Turn-Off Delay from $\overline{SET}$ or $\overline{RESET}$	t_{pd+}*	0.8 V	5.0 V	5.0 V	Gnd	Gnd	A	B	C	D	–	50	ns
Turn-On Delay from Clock	t_{pd-}	E	2.4 V	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	10	50	ns
Turn-Off Delay from Clock	t_{pd+}	E	2.4 V	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	10	50	ns
Minimum Input Setup Time at J*	t_{Setup}**	E	2.4 V	2.4 V	F	Gnd	5.0 V	5.0 V	H,I	H,I	–	20	ns
Minimum Input Hold Time at J1, J2	t_{Hold}**	E	G	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	–	5	ns

†Output shall toggle with each input pulse
*$\overline{SET}$ or $\overline{RESET}$ function can occur only when clock input is low. Other gates are inhibited.
**Identical test to be performed on K* Input.

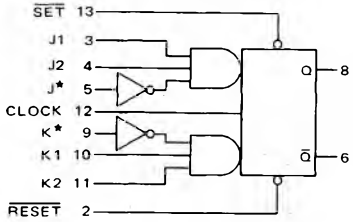
VOLTAGE WAVEFORMS AND DEFINITIONS



††PRF varies when testing f_{Tog}.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
									mA		Volts							
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}
								MC5470	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
								MC7470	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

Characteristic		Symbol	Pin Under Test	MC5470 Test Limits -55 to +125°C Min	Max	Unit	MC7470 Test Limits 0° to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current**	J	I_F	3	–	-1.6	mAdc	–	-1.6	mAdc	–	–	3	–	–	2*,4,10,11	–	–	–	14	5,7,9
	K		10	–	-1.6		–	-1.6		–	–	10	–	–	3,4,11,13*	–	–	–		
	$\overline{Set}$		13	–	-3.2		–	-3.2		–	–	13	–	–	3,4,10,11	–	–	–		
	$\overline{Reset}$		2	–	-3.2		–			–	–	2	–	–	3,4,10,11	–	–	–		
	Clock		12	–	-1.6		–			–	–	12	–	–	2*,3,4,10,11	–	–	–		
			12	–	-1.6		–			–	–	12	–	–	3,4,10,11,13*	–	–	–		
Leakage Current**	J	I_{R1}	3	–	40	μAdc	–	40	μAdc	–	–	–	3	–	5	–	–	–	14	2,4,7
	K		10	–	40		–	40		–	–	–	10	–	9	–	–	–		7,11,13
	$\overline{Set}$		13	–	80		–	80		–	–	–	13	–	9	–	–	–		7,10,11
	$\overline{Reset}$		2	–	80		–	80		–	–	–	2	–	5	–	–	–		7,10,11
	Clock		12	–	40		–	40		–	–	–	12	–	–	–	–	–		3,4,7
	J	I_{R2}	3	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	3	5	–	–	–	14	2,4,7
	K		10	–			–			–	–	–	–	10	9	–	–	–		7,11,13
	$\overline{Set}$		13	–			–			–	–	–	–	13	9	–	–	–		7,10,11
	$\overline{Reset}$		2	–			–			–	–	–	–	2	5	–	–	–		7,10,11
	Clock		12	–			–			–	–	–	–	12	–	–	–	–		7
Output																				
Output Voltage		V_{OL}	6	–	0.4	Vdc	–	0.4	Vdc	6	–	–	–	–	–	2	13	14	–	7,12
			8	–	0.4	Vdc	–	0.4	Vdc	8	–	–	–	–	–	13	2	14	–	7,12
		V_{OH}	6	2.4	–	Vdc	2.4	–	Vdc	–	6	–	–	–	–	13	2	14	–	7,12
			8	2.4	–	Vdc	2.4	–	Vdc	–	8	–	–	–	–	2	13	14	–	7,12
Short-Circuit Current		I_{SC}	6	-20	-57	mAdc	-18	-57	mAdc	–	–	13	–	–	–	–	–	–	14	5,7,9,12
			8	-20	-57	mAdc	-18	-57	mAdc	–	–	2	–	–	–	–	–	–	14	5,7,9,12
Power Requirements																				
Power Supply Drain		I_{PD}	14	–	26	mAdc	–	26	mAdc	–	–	–	–	–	–	–	–	–	14	2,7,12
			14	–	26	mAdc	–	26	mAdc	–	–	–	–	–	–	–	–	–	14	7,12,13

*Momentarily ground pin prior to taking measurement.
**When testing J* or K* other inputs are left open.