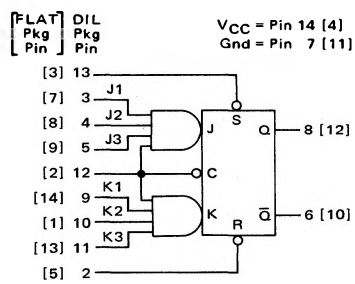
J-K FLIP-FLOP

MC5472 • MC7472

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7472 only.



J = J1 • J2 • J3
K = K1 • K2 • K3

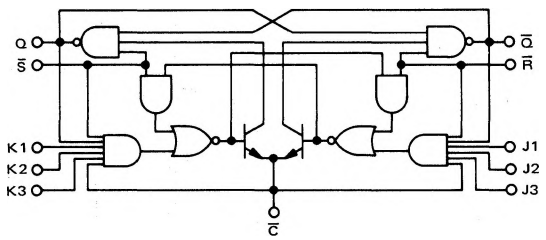
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
$\overline{\text{Clock}}$, $\overline{\text{Set}}$, $\overline{\text{Reset}}$ = 2

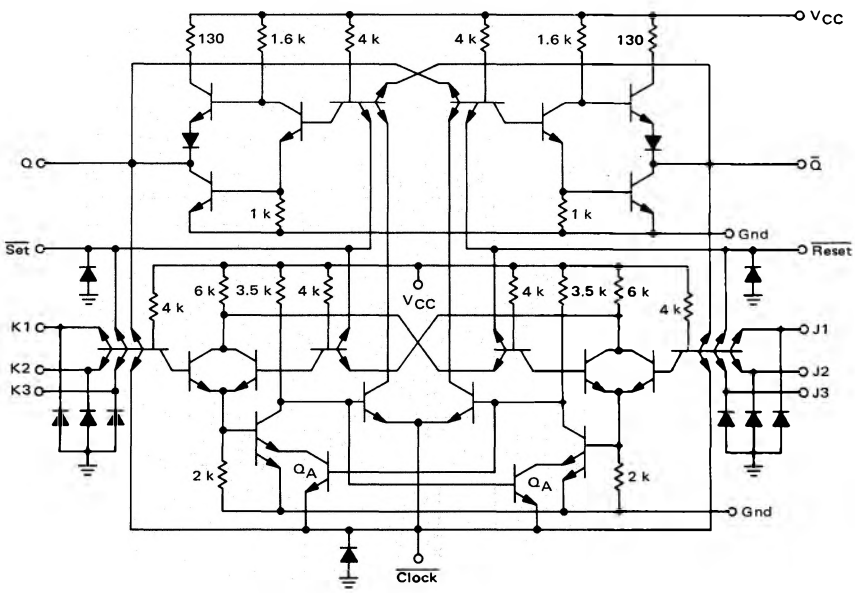
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 20 MHz typ

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs.

LOGIC DIAGRAM

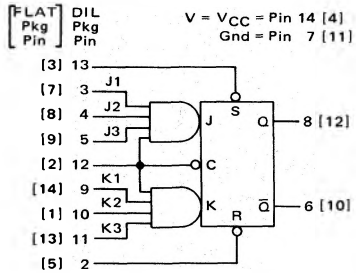


CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{Set}$, $\overline{Reset}$, and $\overline{Clock}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
MC5472	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50	Pin 7[11] is grounded for all tests in addition to the pins listed below:
MC7472	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25	

Characteristic		Symbol	Pin Under Test	MC5472 Test Limits −55 to +125°C Min	Max	Unit	MC7472 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	J	I_F	J1	-	-1.6	mAdc	-	-1.6	mAdc	-	-	J1	-	-	C,J2,J3,R*	-	-	-	-	V	-
	K		K1	-	-1.6		-	-1.6		-	-	K1	-	-	C,K2,K3,S*	-	-	-	-		-
	$\overline{Set}$		S	-	-3.2		-	-3.2		-	-	S	-	-	C,J1,J2,J3,K1,K2,K3	-	-	-	-		-
	$\overline{Reset}$		R	-	↓		-	↓		-	-	R	-	-	C,J1,J2,J3,K1,K2,K3	-	-	-	-		-
	$\overline{Clock}$		C	-			-			-	-	C	-	-	J1,J2,J3,K1,K2,K3,R*	-	-	-	-		-
			C	-	↓	↓	-	↓	↓	-	-	C	-	-	J1,J2,J3,K1,K2,K3,S*	-	-	-	-	↓	-
Leakage Current	J	I_{R1}	J1	-	40	μAdc	-	40	μAdc	-	-	-	J1	-	-	-	-	-	-	V	C,J2,J3,R
	K		K1	-	40		-	40		-	-	-	K1	-	-	-	-	-	-		C,K2,K3,S
	$\overline{Set}$		S	-	80		-	80		-	-	-	S	-	-	-	-	-	-		C,J1,J2,J3
	$\overline{Reset}$		R	-	↓		-	↓		-	-	-	R	-	-	-	-	-	-		C,K1,K2,K3
	$\overline{Clock}$		C**	-			-			-	-	-	C	-	-	-	-	-	-		C,J1,J2,J3,K1,K2,K3,R
	J	I_{R2}	J1	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	J1	-	-	-	-	-	V	C,J2,J3,R
	K		K1	-			-			-	-	-	-	K1	-	-	-	-	-		C,K2,K3,S
	$\overline{Set}$		S	-			-			-	-	-	-	S	-	-	-	-	-		C,J1,J2,J3
	$\overline{Reset}$		R	-			-			-	-	-	-	R	-	-	-	-	-		C,K1,K2,K3
	$\overline{Clock}$		C	-	↓	↓	-	↓	↓	-	-	-	-	C	-	-	-	-	-	↓	C,J1,J2,J3,K1,K2,K3,S
Output																					
Output Voltage		V_{OL}	$\bar{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\bar{Q}$	-	-	-	-	-	R	S	-	V	-	-
			Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	S	R	-	V	-	-
		V_{OH}	$\bar{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\bar{Q}$	-	-	-	-	S	R	-	V	-	-
			Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	R	S	-	V	-	-
Short-Circuit Current		I_{SC}†	$\bar{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	J1,J2,J3,K1,K2,K3	-	-	-	-	V	C,$\bar{Q}$,R
			Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	J1,J2,J3,K1,K2,K3	-	-	-	-	V	C,Q,S
Power Requirements																					
Power Supply Drain		I_{PD}	V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	V	-	-	R
			V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	V	-	-	S

*Momentarily ground pin prior to taking measurement.
**Under normal operating conditions this current is negative.
†Only one output should be shorted at a time.
This test guarantees that positive leakage current will not exceed the limit shown.

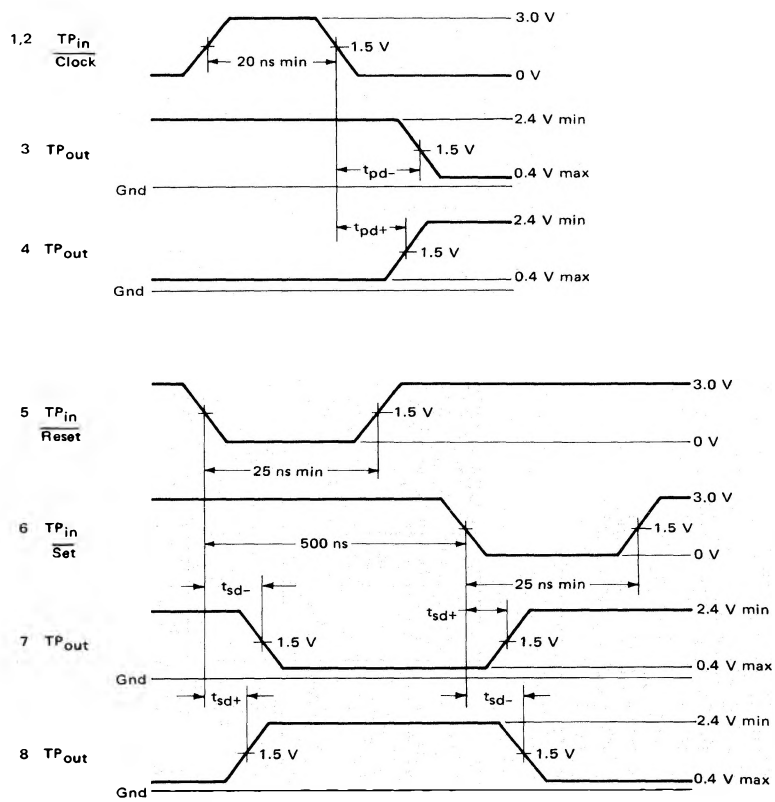
TEST PROCEDURES

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	1	2.4 V	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	2	2	2.4 V	2.4 V	3	3	10	40	ns
Turn-Off Delay	t_{pd+}	2	2	2.4 V	2.4 V	4	4	10	25	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	5	6	7	8	–	40	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	5	6	7	8	–	25	ns
Enable Voltage	V_{EN}	2	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	2	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS

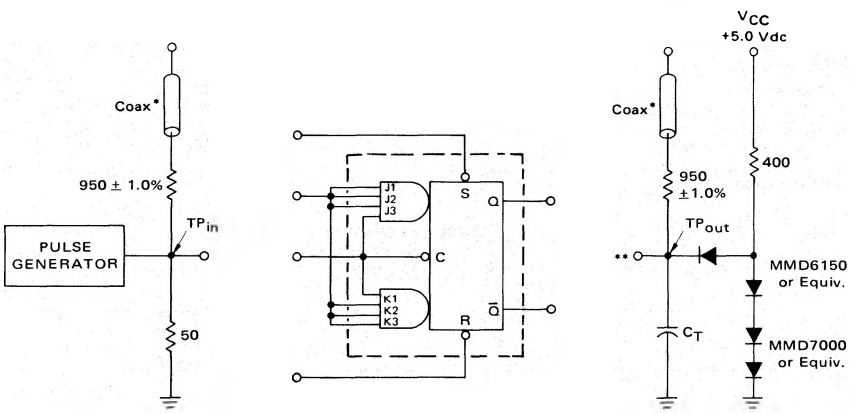
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{Reset}}$ input will force the Q output to the logic "1" state. The $\overline{\text{Reset}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of −2.0 V appear at the clock.

SWITCHING TIME TEST CIRCUIT



t+ = 10 ns
t− = 5 ns
PRF = 15 MHz for waveform 1
1.0 MHz for waveforms 2, 5, and 6

Two pulse generators are required and must be slaved together for testing $\overline{\text{Set}}$ and $\overline{\text{Reset}}$. Only one pulse generator is required for J, K, and Clock tests.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.