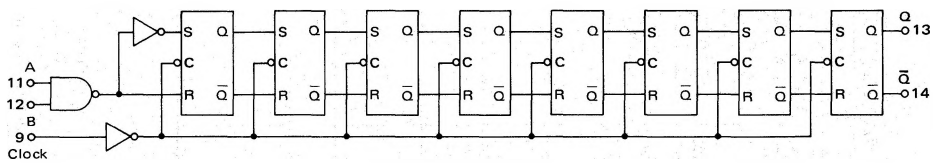
MC5491AL*
MC7491AL,P*

The 8-bit serial-in, serial-out shift register is composed of eight R-S master-slave flip-flops, an input AND gate, and a clock driver.

Single rail data inputs are ANDed together and applied to the input of the first flip-flop. The clock inverter-driver is common to all eight flip-flops and causes information to be shifted to the output on the positive edge of the input clock pulse. Both Q and $\overline{Q}$ are available from the last bit.

The 8-bit shift register may be used as an 8-bit delay line in data handling systems and control systems.



V_{CC} = Pin 5
Gnd = Pin 10

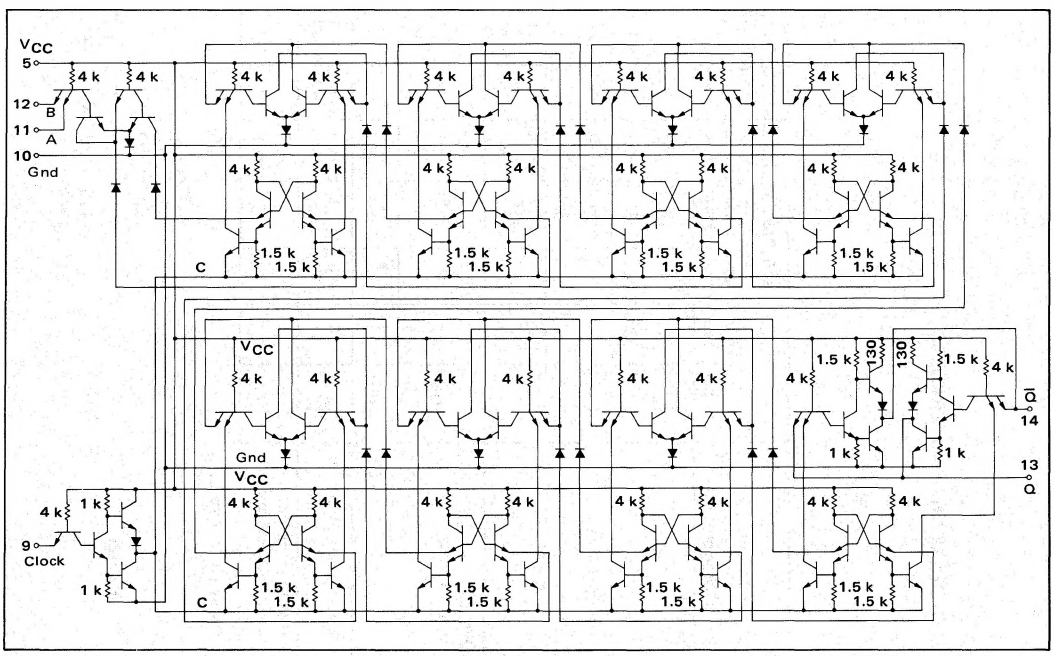
TRUTH TABLE

Synchronous Inputs

t_n		t_{n+8}	
A	B	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 175 mW typ/pkg
Propagation Delay Time = 25 ns typ
Operating Frequency = 18 MHz typ



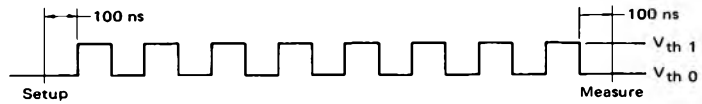
*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

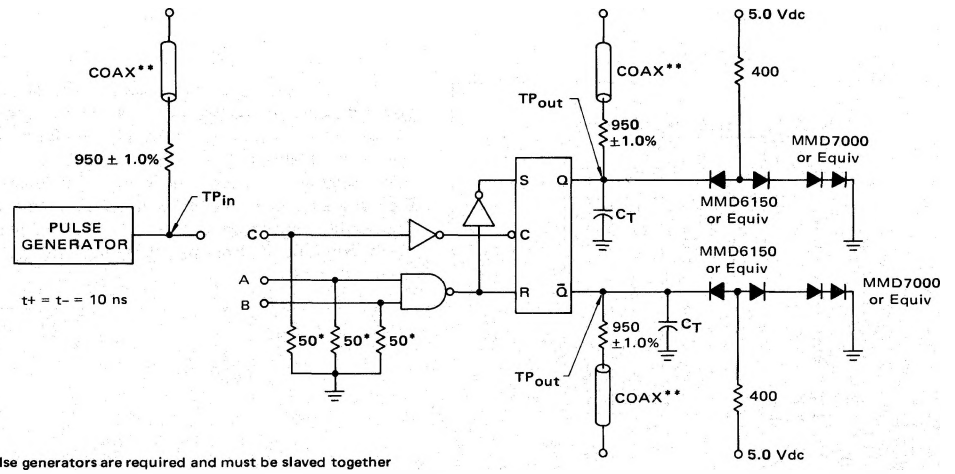
									TEST CURRENT / VOLTAGE VALUES (All Temperatures)											
									mA		Volts									
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	
									MC5491A											
									16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.5	5.5	
									MC7491A											
									16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.75	5.25	
			MC5491A Test Limits −55 to +125°C			MC7491A Test Limits 0 to +70°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	**	Gnd
Input																					
Forward Current	I_F	9	-	-1.6	mAdc	-	-1.6	mAdc	-	-	9	-	-	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	11	-	-	12	-	-	-	-	↓	-	↓
		12	-			-			-	-	12	-	-	11	-	-	-	-		-	
Leakage Current	I_{R1}	9	-	40	μAdc	-	40	μAdc	-	-	-	9	-	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	-	11	-	-	-	-	-	-	↓	-	10,12
		12	-			-			-	-	-	12	-	-	-	-	-	-		-	10,11
	I_{R2}	9	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	9	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	-	-	11	-	-	-	-	-	↓	-	10,12
		12	-			-			-	-	-	-	12	-	-	-	-	-		-	10,11
Output																					
Output Voltage	V_{OL}	13	-	0.4	Vdc	-	0.4	Vdc	13	-	-	-	-	-	-	-	11,12	5	-	9	10
		13	-	↓	↓	-	↓	↓	13	-	-	-	-	-	-	12	11	↓	-	↓	↓
		14	-			-			14	-	-	-	-	-	-	11,12	-		-		
	V_{OH}	13	2.4	-	Vdc	2.4	-	Vdc	-	13	-	-	-	-	-	11,12	-	5	-	9	10
		14	2.4	-	Vdc	2.4	-	Vdc	-	14	-	-	-	-	-	11	12	5	-	9	10
Short-Circuit Current	I_{SC}	13	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	-	9,10,11,12,13,14
		14	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	-	9,10,11,12,13,14
Power Requirements																					
Power Supply Drain	I_{PD}	10	-	50*	mAdc	-	58*	mAdc	-	-	-	-	-	-	-	-	-	-	5	9	10,11,12

*Tested only at 25°C.

**Input pulse:



SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together to provide the waveforms shown. Pulse generator for Pulses A and B must be operated in the double pulse mode.

*Resistor used only when that input is under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

TEST	INPUT			Q	Q̄	LIMITS		
	B	A	C			Min	Max	Unit
f_{Tog}	W	W	T	*	–	10	–	MHz
t_{pd+}	V	2.4 V	U	Y	–	–	40	ns
t_{pd+}	2.4 V	V	U	–	Y	–	40	ns
t_{pd-}	2.4 V	X	U	Z	–	–	40	ns
t_{pd-}	X	2.4 V	U	–	Z	–	40	ns

*Output shall toggle with each input pulse.

VOLTAGE WAVEFORMS AND DEFINITIONS

Pulse T: f = 10 MHz, Duty Cycle = 50%
Pulse U: f = 1.0 MHz, Duty Cycle = 50%
Pulse V: f = 0.5 MHz
Pulse W: f = 5.0 MHz
Pulse X: f = 0.5 MHz
Pulse Y: TP_{out}
Pulse Z: $\overline{TP_{out}}$