4-BIT BINARY COUNTER

MC5493L*
MC7493L,P*

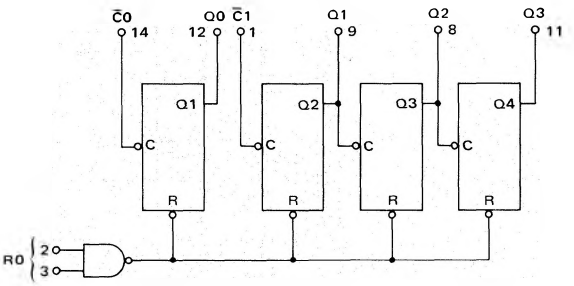
This 4-bit counter is comprised of two sections: a divide-by-two section and a divide-by-eight section. These sections can be used independently, or can be connected to provide the divide-by-16 function. All outputs of the counter can be set to the logic "0" state by applying a logic "1" level to the Reset input.

TRUTH TABLE

Connect Q0 to $\overline{C}1$

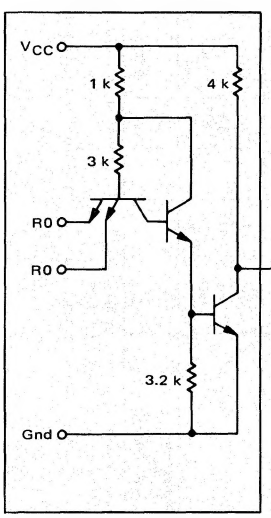
	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Input Loading Factor
R0 = 1
$\overline{C}0$, $\overline{C}1$ = 2
Output Loading Factor = 10
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 20 ns typ/bit

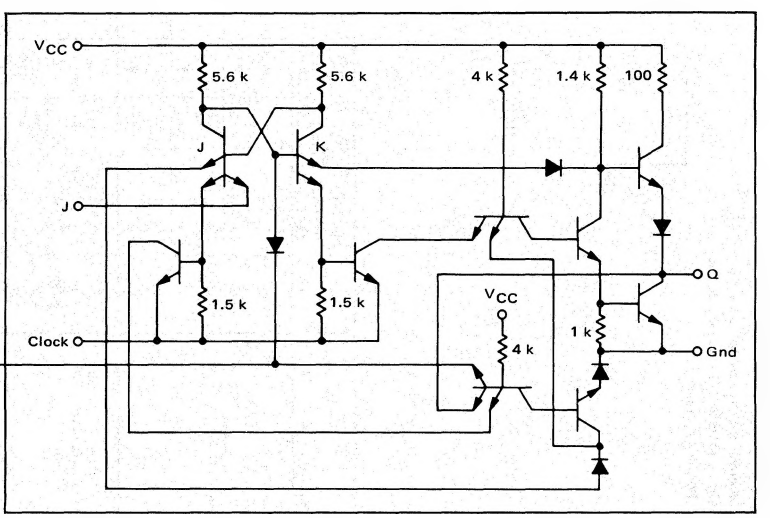


V_{CC} = Pin 5
Gnd = Pin 10

RESET GATE



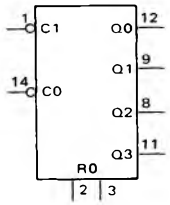
TYPICAL FLIP-FLOP



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the reset gate. The other input is tested in the same manner.

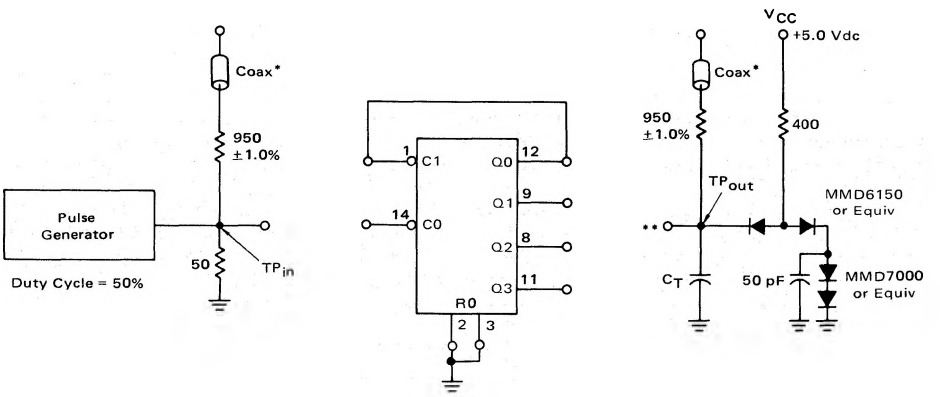


									TEST CURRENT/VOLTAGE VALUES (All Temperatures)														
									mA		Volts												
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CCL}	V_{CCH}				
									MC5493	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.7	4.5	5.5			
									MC7493	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.8	4.75	5.25			
				MC5493 Test Limits -55 to +125°C			MC7493 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													
Characteristic		Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																							
Forward Current	R0	I_F	2	–	-1.6	mAdc	–	-1.6	mAdc	–	–	2	–	–	3	–	–	–	–	5	–	10
	$\bar{C}0$		14	–	-3.2	↓	–	-3.2	↓	–	–	14	–	–	–	–	–	–	–	↓	–	–
	$\bar{C}1$		1	–	-3.2		–	-3.2		–	–	1	–	–	–	–	–	–	–		–	↓
Leakage Current	R0	I_{R1}	2	–	40	μAdc	–	40	μAdc	–	–	–	2	–	–	–	–	–	–	5	–	3,10
	$\bar{C}0$		14	–	80	↓	–	80	↓	–	–	–	14	–	–	–	–	–	–	↓	–	10
	$\bar{C}1$		1	–	80		–	80		–	–	–	1	–	–	–	–	–	–		–	10
	R0	I_{R2}	2	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	2	–	–	–	–	–	5	–	3,10
	$\bar{C}0$		14	–	↓	↓	–	↓	↓	–	–	–	–	14	–	–	–	–	–	↓	–	10
	$\bar{C}1$		1	–			–			–	–	–	–	1	–	–	–	–	–		–	10
Output																							
Output Voltage	Q0 ①	V_{OL}	12	–	0.4	Vdc	–	0.4	Vdc	12	–	–	–	–	–	2,3	–	–	5	–	–	10
Short-Circuit Current		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	14	–	5	14	2,3,10,12
Output Voltage		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	12	–	–	–	–	–	2,3	14	5	–	–	10
	Q1 ①	V_{OL}	9	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	–	–	2,3	–	–	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	1	–	5	1	2,3,9,10
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	9	–	–	–	–	–	2,3	1	5	–	–	10
	Q2 ①	V_{OL}	8	–	0.4	Vdc	–	0.4	Vdc	8	–	–	–	–	–	2,3	–	1	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	↓	–	5	5	2,3,8,10
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	8	–	–	–	–	–	2,3		5	–	–	10
	Q3 ①	V_{OL}	11	–	0.4	Vdc	–	0.4	Vdc	11	–	–	–	–	–	2,3	–	1	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	↓	–	5	1	2,3,10,11
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	11	–	–	–	–	–	2,3		5	–	–	10
Power Requirements (Total Device)																							
Power Supply Drain		I_{PD}	5	–	46	mAdc	–	53	mAdc	–	–	–	–	–	–	–	–	–	–	5	–	10

Pulse 1: Apply positive pulse prior to taking measurement to set the device in the desired state. Maintain $V_{th\ L}$ voltage for measurement.

① All input, power supply and ground voltages must be maintained between each test unless otherwise noted.

SWITCHING TIME TEST CIRCUIT



f_{Tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

VOLTAGE WAVEFORMS AND DEFINITIONS