MC74HC4351

Analog Multiplexers/ Demultiplexers with Address Latch

High−Performance Silicon−Gate CMOS

The MC54/74HC4351, and MC54/74HC4353 utilize silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel−Select inputs may be latched by using the active−low Latch Enable pin. When Latch Enable is high, the latch is transparent. When either Enable 1 (active low) or Enable 2 (active high) is inactive, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

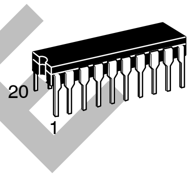
These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal−gate CMOS analog switches.

For multiplexers/demultiplexers without latches, see the HC4051, HC4052, and HC4053.

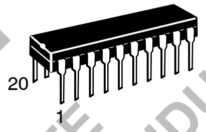
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} − V_{EE}) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC} − GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal−Gate Types
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4351 — 222 FETs or 55.5 Equivalent Gates
  HC4353 — 186 FETs or 46.5 Equivalent Gates

ON Semiconductor®

http://onsemi.com



J SUFFIX
CERAMIC PACKAGE
CASE 732−03



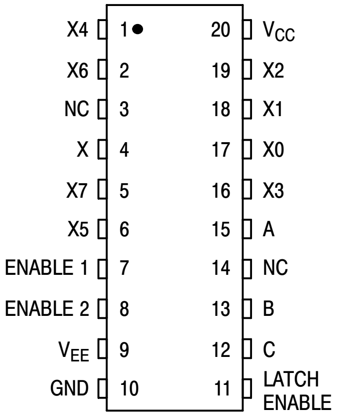
N SUFFIX
PLASTIC PACKAGE
CASE 738−03

DW SUFFIX
SOIC PACKAGE
CASE 751D−04

ORDERING INFORMATION

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXDW	SOIC

PIN ASSIGNMENT
MC54/74HC4351

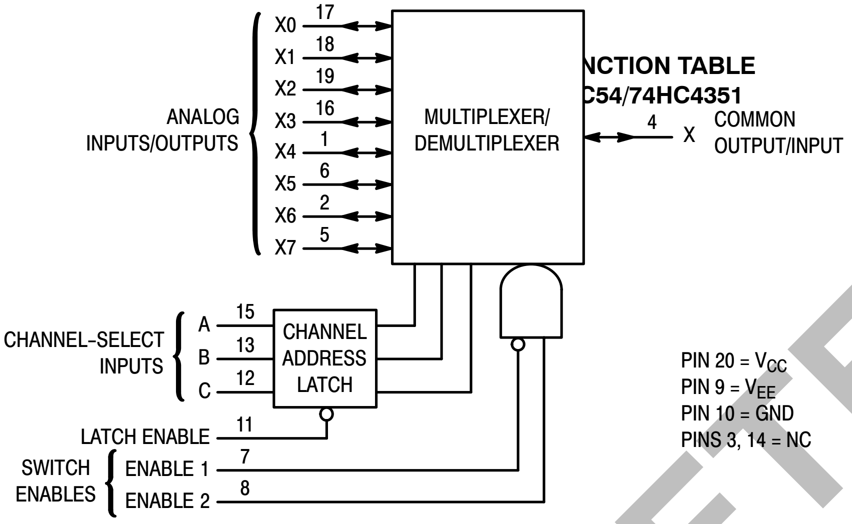


NC = NO CONNECTION

June, 2006 − Rev. 7

Publication Order Number:
MC74HC4351/D

LOGIC DIAGRAM
MC54/74HC4351
Single−Pole, 8−Position Plus Common Off and Address Latch



PIN 20 = V_{CC}
PIN 9 = V_{EE}
PIN 10 = GND
PINS 3, 14 = NC

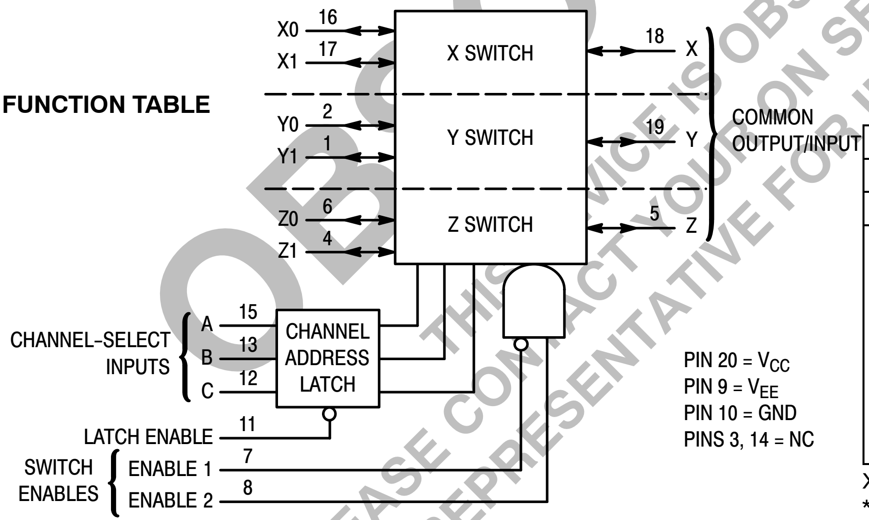
NCTION TABLE
C54/74HC4351

Control Inputs					ON Channel (LE = H)*
Enable		Select			
1	2	C	B	A	
L	H	L	L	L	X0
L	H	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	H	H	L	L	X4
L	H	H	L	H	X5
L	H	H	H	L	X6
L	H	H	H	H	X7
H	X	X	X	X	None
X	L	X	X	X	None

X = don't care

*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

BLOCK DIAGRAM
MC54/74HC4353
Triple Single−Pole, Double−Position Plus Common Off and Address Latch

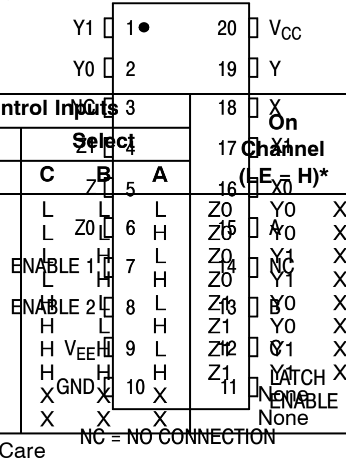


PIN 20 = V_{CC}
PIN 9 = V_{EE}
PIN 10 = GND
PINS 3, 14 = NC

NOTE:

This device allows independent control of each switch. Channel−Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

PIN ASSIGNMENT



NC = NO CONNECTION

FUNCTION TABLE

Control Inputs					On Channel (LE = H)*		
Enable		Select					
1	2	C	B	A			
L	H	L	L	L	Z0	Y0	X0
L	H	L	L	H	Z0	Y0	X1
L	H	L	H	L	Z0	Y1	X0
L	H	L	H	H	Z0	Y1	X1
L	H	H	L	L	Z1	Y0	X0
L	H	H	L	H	Z1	Y0	X1
L	H	H	H	L	Z1	Y1	X0
L	H	H	H	H	Z1	Y1	X1
H	X	X	X	X	None		
X	L	X	X	X	None		

X = Don't Care

*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)	– 1.5 to V_{CC} + 1.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air,Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated. See Applications Information.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 6.0	GND	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, Channel Select or Enable Inputs (Figure 9a) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{in}	Maximum Input Leakage Current, Channel−Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enables = V_{CC} or GND V_{IS} = V_{CC} or GND V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 2 8	 20 80	 40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
R_{on}	Maximum “ON” Resistance	$V_{in} = V_{IL}$ or V_{IH}	4.5	0.0	190	240	280	Ω
		$V_{IS} = V_{CC}$ to V_{EE}	4.5	– 4.5	120	150	170	
		$I_S \leq 2.0$ mA (Figures 1, 2)	6.0	– 6.0	100	125	140	
		$V_{in} = V_{IL}$ or V_{IH}	4.5	0.0	150	190	230	
		$V_{IS} = V_{CC}$ or V_{EE} (Endpoints)	4.5	– 4.5	100	125	140	
		$I_S \leq 2.0$ mA (Figures 1, 2)	6.0	– 6.0	80	100	115	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH}	4.5	0.0	30	35	40	Ω
		$V_{IS} = 1/2 (V_{CC} - V_{EE})$	4.5	– 4.5	12	15	18	
		$I_S \leq 2.0$ mA	6.0	– 6.0	10	12	14	
I_{off}	Maximum Off−Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} - V_{EE}$ Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	µA
	Maximum Off−Channel Leakage Current, Common Channel HC4351	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} - V_{EE}$ Switch Off (Figure 4)	6.0	– 6.0	0.2	2.0	4.0	
	HC4353		6.0	– 6.0	0.1	1.0	2.0	
I_{on}	Maximum On−Channel Leakage Current, Channel to Channel HC4351	$V_{in} = V_{IL}$ or V_{IH} Switch to Switch = $V_{CC} - V_{EE}$ (Figure 5)	6.0	– 6.0	0.2	2.0	4.0	µA
	HC4353		6.0	– 6.0	0.1	1.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel−Select to Analog Output (Figure 9)		2.0	370	465	550	ns
			4.5	74	93	110	
			6.0	63	79	94	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)		2.0	60	75	90	ns
			4.5	12	15	18	
			6.0	10	13	15	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Analog Output (Figure 12)		2.0	325	410	485	ns
			4.5	65	82	97	
			6.0	55	70	82	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)		2.0	290	365	435	ns
			4.5	58	73	87	
			6.0	49	62	74	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)		2.0	345	435	515	ns
			4.5	69	87	103	
			6.0	59	74	87	
C_{in}	Maximum Input Capacitance		—	10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O	Enable 1 = V_{IH}, Enable 2 = V_{IL}	—	35	35	35	pF
	Common O/I: HC4351		—	130	130	130	
	HC4353			50	50	50	
	Feedthrough		—	1.0	1.0	1.0	

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package) (Figure 14)*	45 (HC4351) 45 (HC4353)	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}{}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Channel−Select to Latch Enable (Figure 12)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Enable to Channel Select (Figure 12)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 12)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times, Channel−Select, Latch Enable, and Enables 1 and 2	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High−Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Condition	V_{CC} V	V_{EE} V	Limit* 25°C 54/74HC			Unit
					51	52	53	
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB $R_L = 50\ \Omega$, $C_L = 10$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	80 80 80	95 95 95	120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} $f_{in} = 10$ kHz, $R_L = 600\ \Omega$, $C_L = 50$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50			dB
		$f_{in} = 1.0$ MHz, $R_L = 50\ \Omega$, $C_L = 10$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40			
—	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	$V_{in} \leq 1$ MHz Square Wave ($t_r = t_f = 6$ ns) Adjust R_L at Setup so that $I_S = 0$ A Enable = GND $R_L = 600\ \Omega$, $C_L = 50$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	25 105 135			mV_{PP}
		$R_L = 10\ k\Omega$, $C_L = 10$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	35 145 190			
—	Crosstalk Between Any Two Switches (Figure 13) (Test does not apply to HC4351)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} $f_{in} = 10$ kHz, $R_L = 600\ \Omega$, $C_L = 50$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50			dB
		$f_{in} = 1$ MHz, $R_L = 50\ \Omega$, $C_L = 10$ pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 60 – 60 – 60			
THD	Total Harmonic Distortion (Figure 15)	$f_{in} = 1$ kHz, $R_L = 10\ k\Omega$, $C_L = 50$ pF THD = $THD_{Measured} - THD_{Source}$ $V_{IS} = 4.0\ V_{PP}$ sine wave $V_{IS} = 8.0\ V_{PP}$ sine wave $V_{IS} = 11.0\ V_{PP}$ sine wave	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.

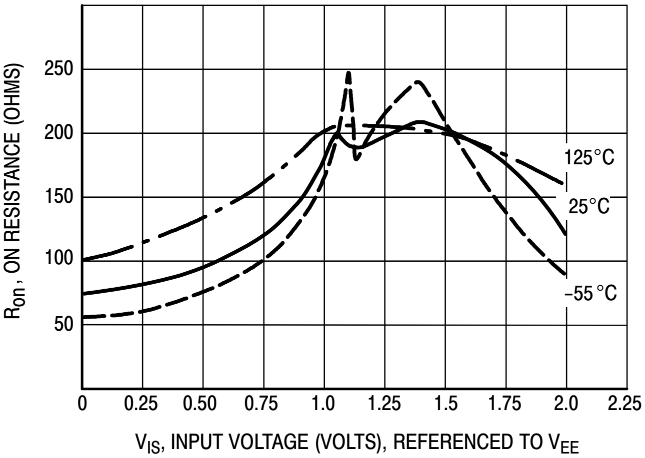


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

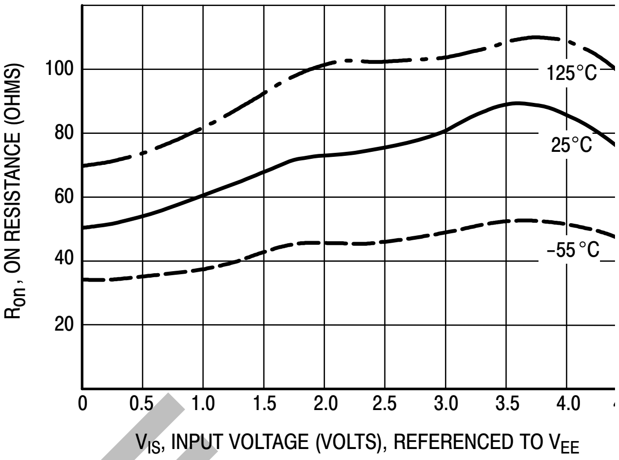


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5

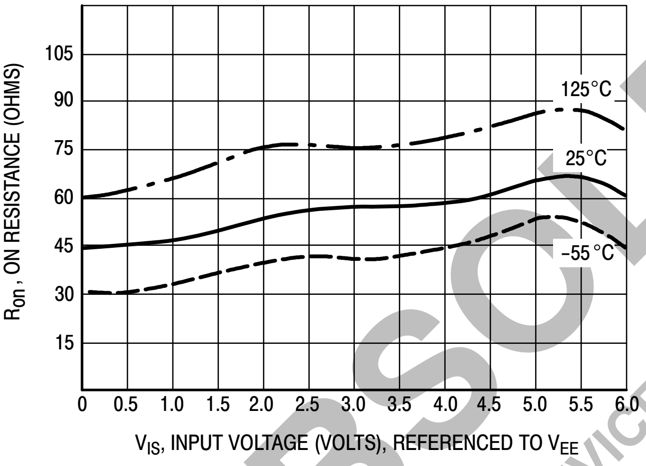


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

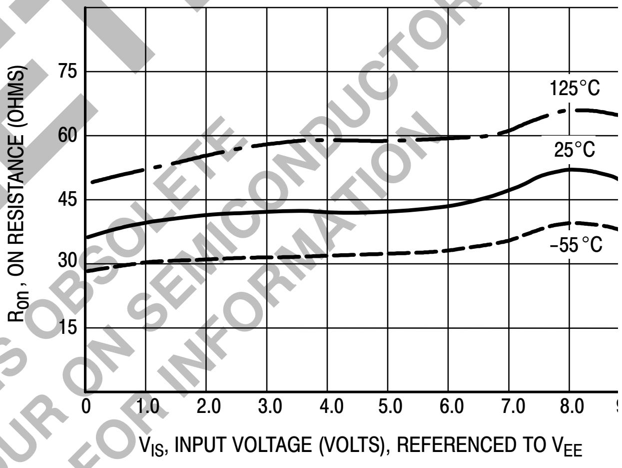


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0

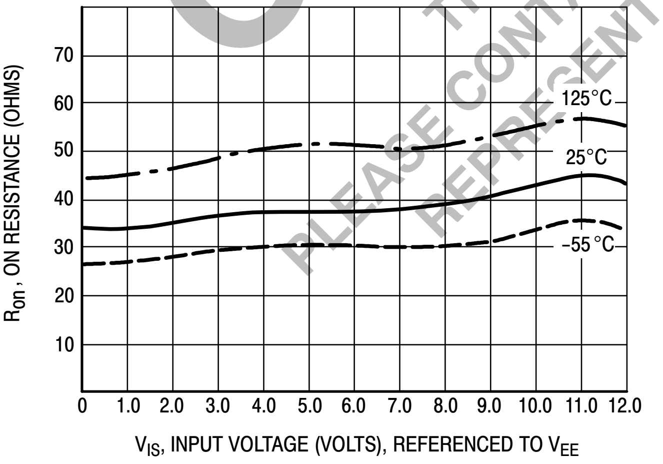


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

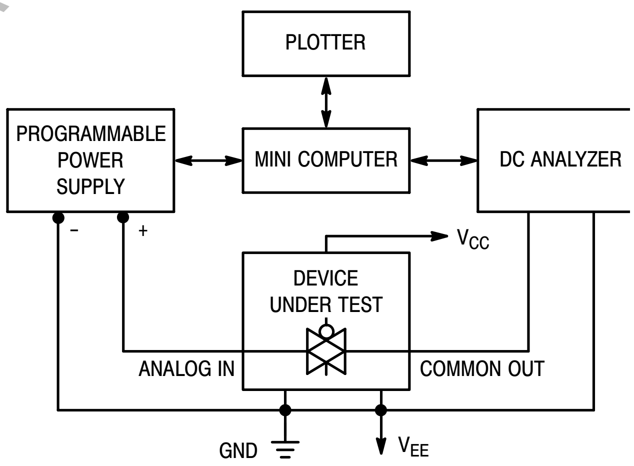


Figure 2. On Resistance Test Set−Up

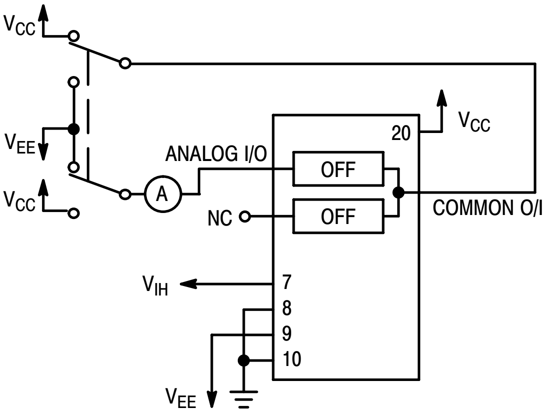


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

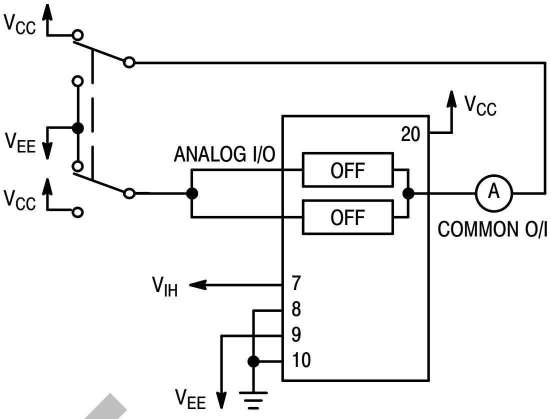


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

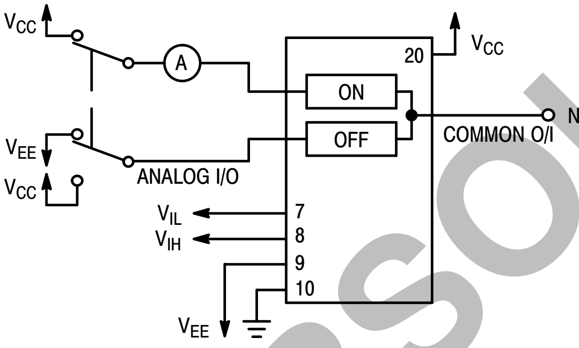
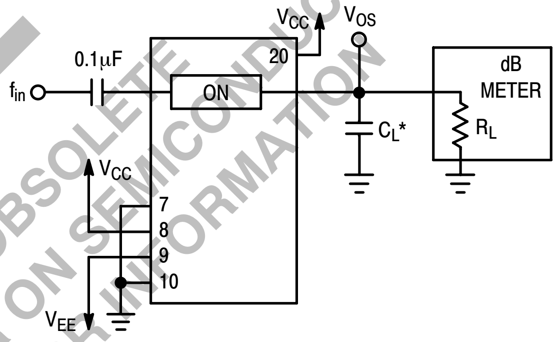
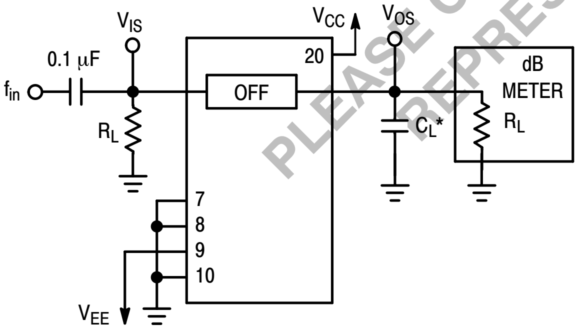


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



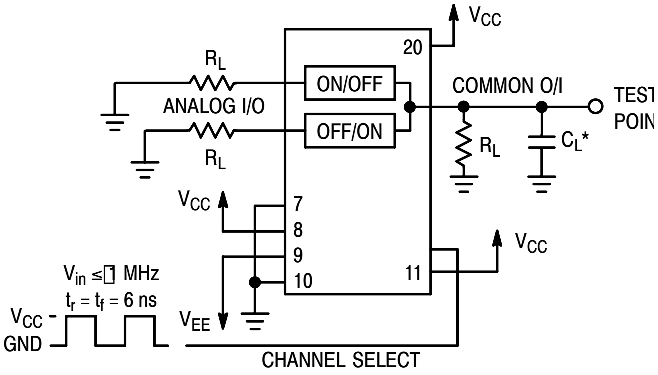
*Includes all probe and jig capacitance.

Figure 6. Maximum On Channel Bandwidth, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Off Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

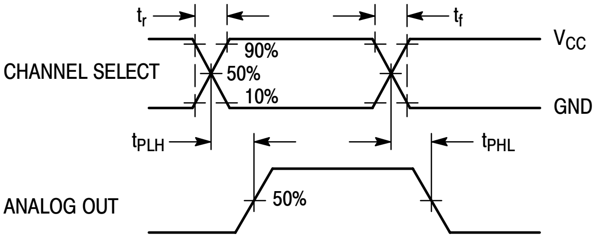
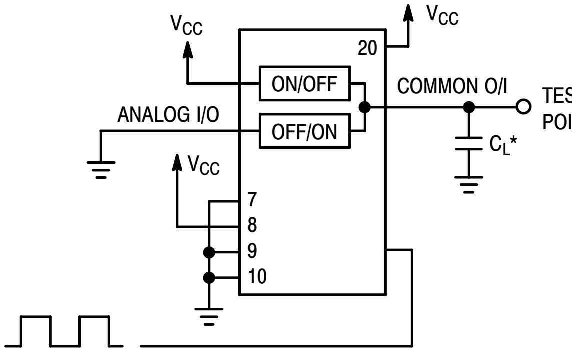


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set−Up Chann Select to Analog Out

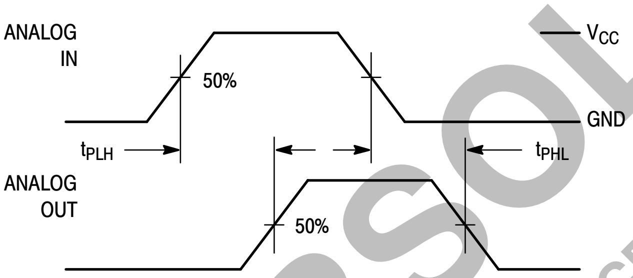
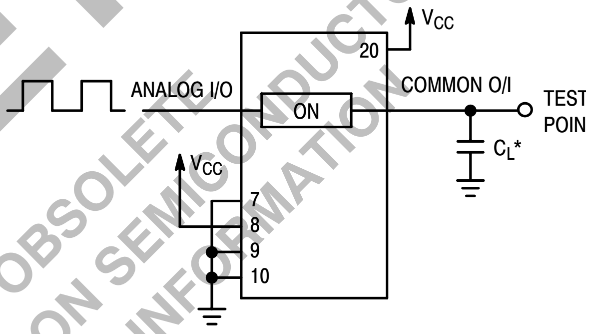


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set−Up Analog In to Analog Out

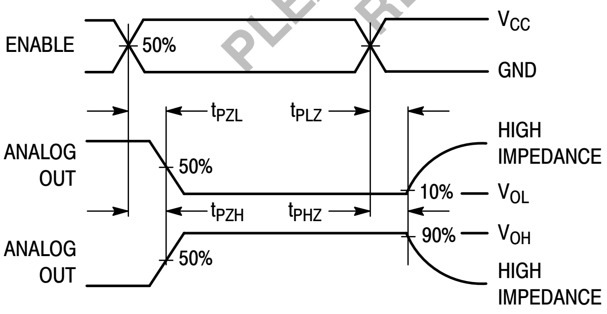


Figure 11a. Propagation Delay, Enable 1 or 2 to Analog Out

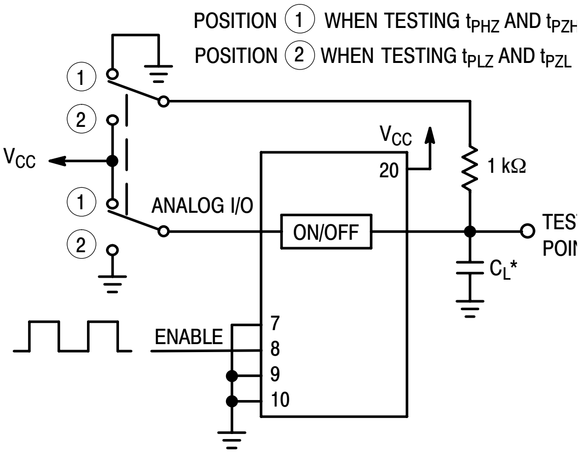


Figure 11b. Propagation Delay, Test Set−Up Enable to Analog Out

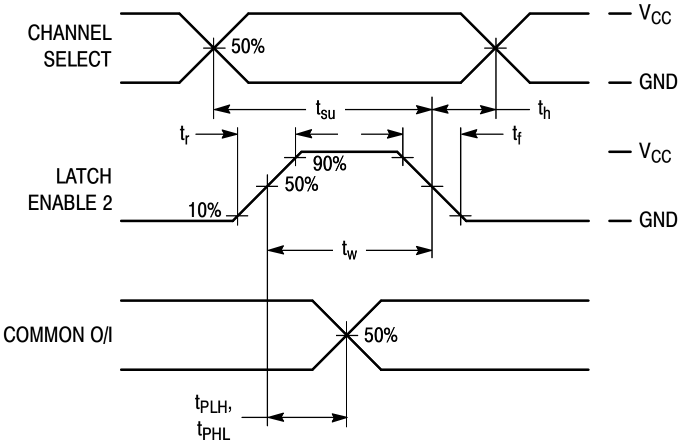
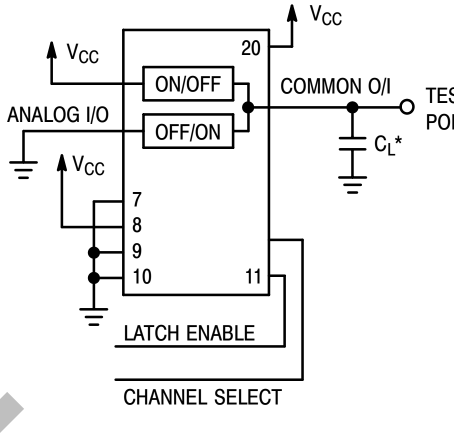
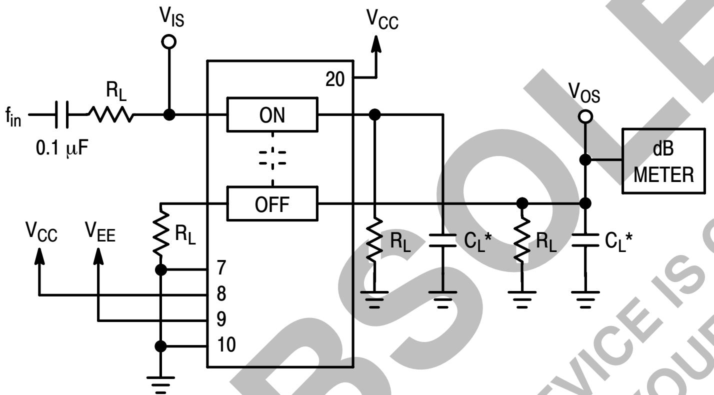


Figure 12a. Propagation Delay, Latch Enable to Analog Out



*Includes all probe and jig capacitance.

Figure 12b. Propagation Delay, Test Set−Up Latch Enable to Analog Out



*Includes all probe and jig capacitance.

Figure 13. Crosstalk Between Any Two Switches, Test Set−Up

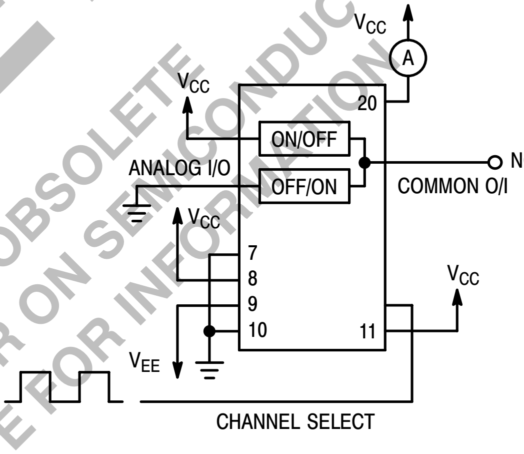
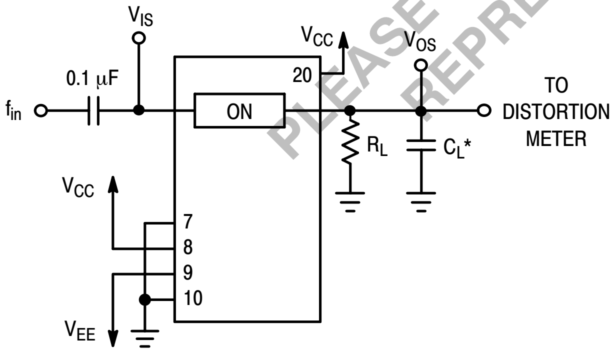


Figure 14. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance.

Figure 15a. Total Harmonic Distortion, Test Set-Up

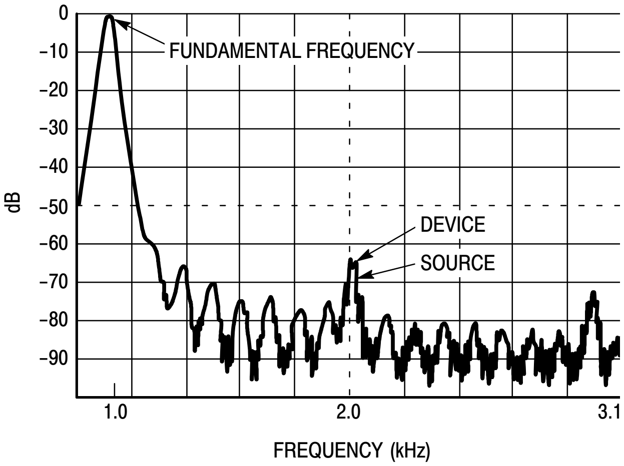


Figure 15b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5\text{ V} = \text{logic high}$$

$$\text{GND} = 0\text{ V} = \text{logic low}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration in Figure 16, a maximum analog signal of ten volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - \text{GND} = 2\text{ to }6\text{ volts}$$

$$V_{EE} - \text{GND} = 0\text{ to }-6\text{ volts}$$

$$V_{CC} - V_{EE} = 2\text{ to }12\text{ volts}$$

$$\text{and } V_{EE} \leq \text{GND}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 17. These diodes should be able to absorb the maximum anticipated current surges during clipping.

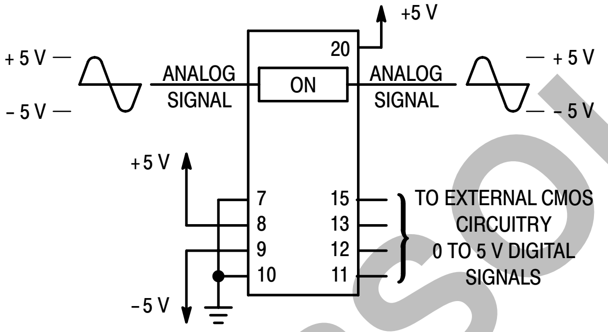


Figure 16. Application Example

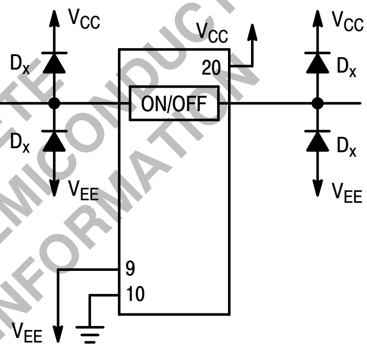
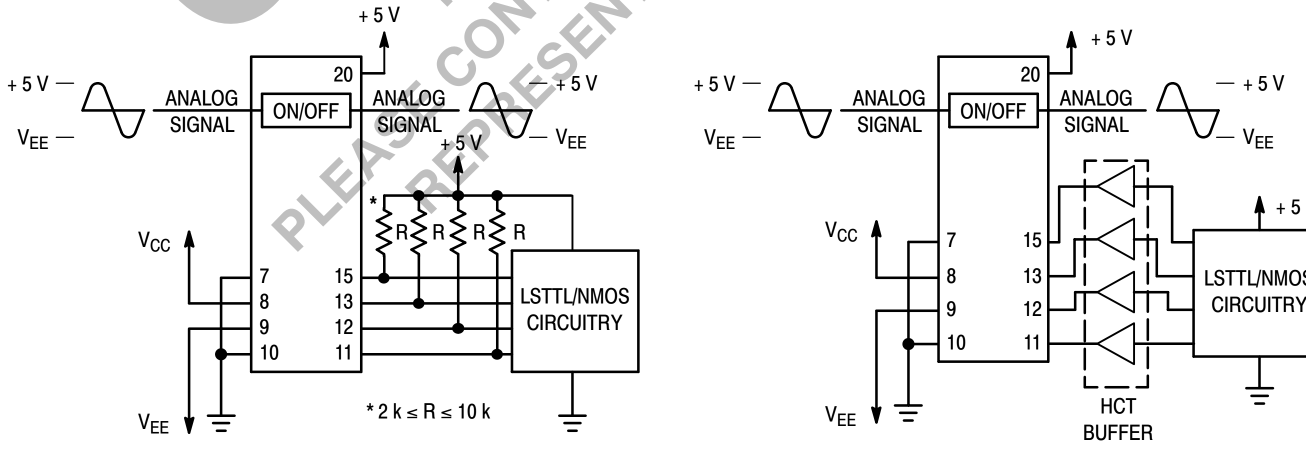


Figure 17. External Germanium or Schottky Clipping Diodes

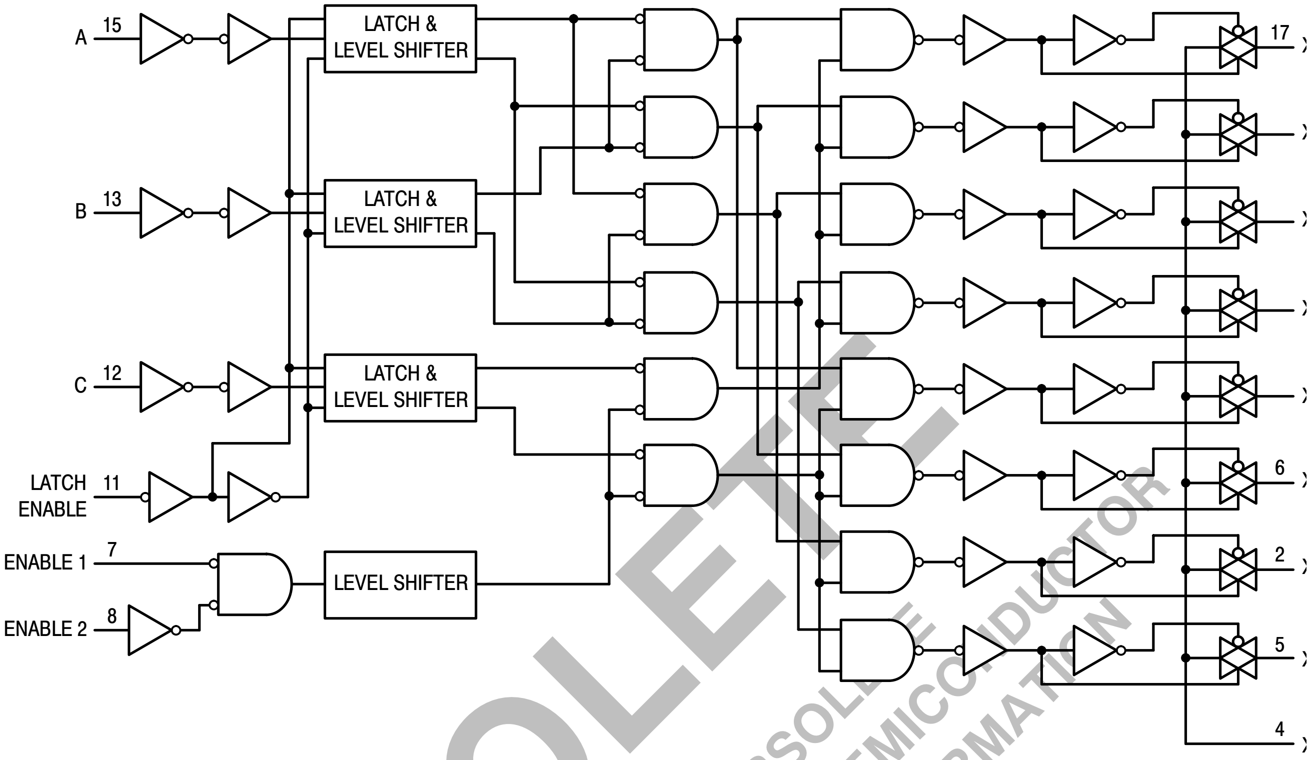


a. Using Pull−Up Resistors

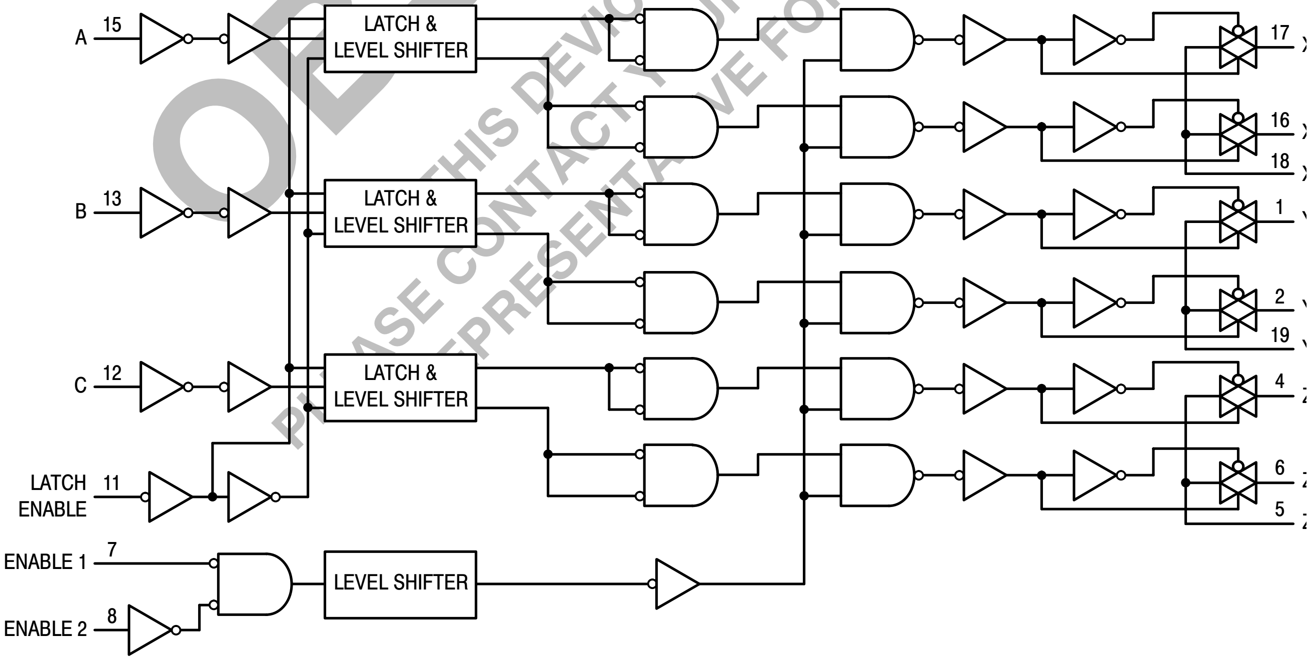
b. Using HCT Interface

Figure 18. Interfacing LSTTL/NMOS to CMOS Inputs

FUNCTION DIAGRAM HC4351

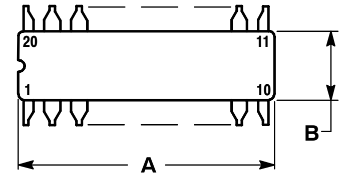


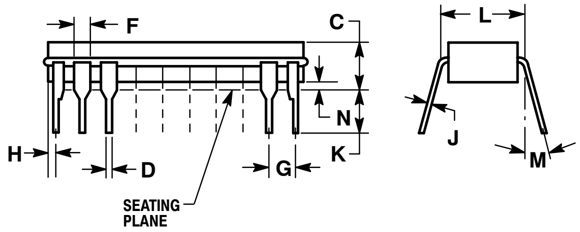
FUNCTION DIAGRAM HC4353



OUTLINE DIMENSIONS

J SUFFIX
CERAMIC PACKAGE
CASE 732−03
ISSUE E

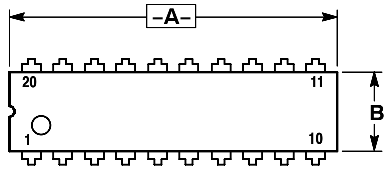


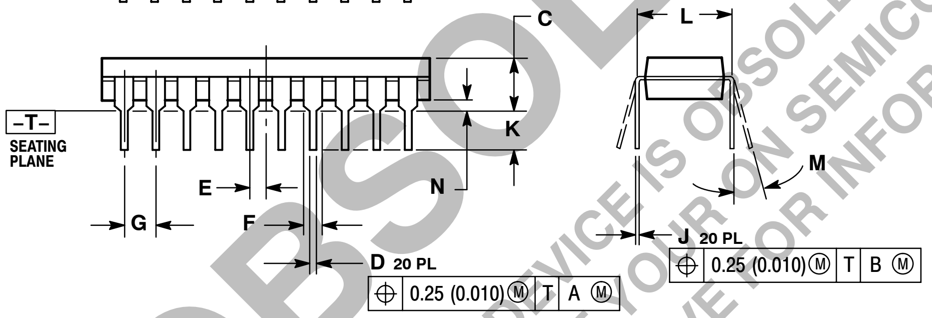


NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

N SUFFIX
PLASTIC PACKAGE
CASE 738−03
ISSUE E

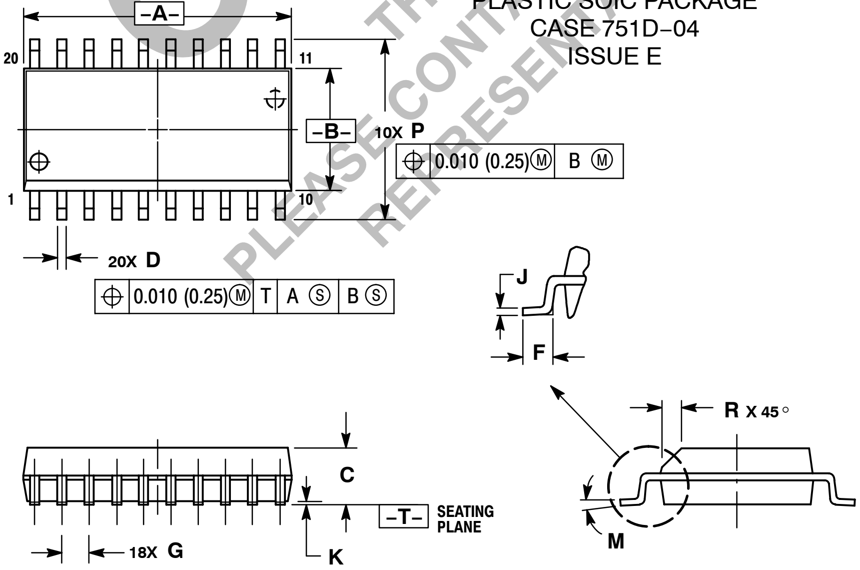




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D−04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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