## **Quad Bus Buffer**

## With 5 V-Tolerant Inputs

The MC74LVX125 is an advanced high speed CMOS quad bus buffer. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The MC74LVX125 requires the 3–state control input  $(\overline{OE})$  to be set High to place the output into the high impedance state.

## **Features**

- High Speed:  $t_{PD} = 4.4 \text{ ns}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu A \text{ (Max)}$  at  $T_A = 25^{\circ}\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V

Machine Model > 200 V

• These Devices are Pb-Free and are RoHS Compliant

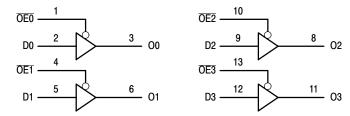


Figure 1. Logic Diagram

#### **PIN NAMES**

Pins	Function
OEn Dn On	Output Enable Inputs Data Inputs 3-State Outputs

## **FUNCTION TABLE**

INPU	JTS	OUTPUTS
<del>OEn</del>	Dn	On
L	L	L
L	Н	Н
Н	X	Z

H= High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for  $I_{\hbox{\scriptsize CC}}$  reasons, DO NOT FLOAT Inputs



## ON Semiconductor®

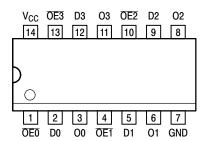
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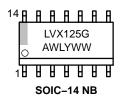
SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

## **PIN ASSIGNMENT**



14-Lead (Top View)

## **MARKING DIAGRAMS**





TSSOP-14

LVX125 = Specific Device Code A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	–0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
l <sub>out</sub>	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>		T <sub>A</sub> = 25°C	;	$T_A = -40$	) to 85°C	
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
l <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μΑ
l <sub>OZ</sub>	Maximum Three–State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	3.6			±0.25		±2.5	μА
Icc	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input $t_f = t_f = 3.0$ ns)

					T <sub>A</sub> = 25°C		$T_A = -40$	) to 85°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Input to Output	V <sub>CC</sub> = 2.7V	$C_L = 15pF$ $C_L = 50pF$		5.8 8.3	10.1 13.6	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		4.4 6.9	6.2 9.7	1.0 1.0	8.5 12.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time OE to O	$V_{CC} = 2.7V$ $R_L = 1k\Omega$	$C_L = 15pF$ $C_L = 50pF$		5.3 7.8	9.3 12.8	1.0 1.0	12.5 16.0	ns
		$\begin{aligned} &V_{CC} = 3.3 \pm 0.3 V \\ &R_L = 1 k \Omega \end{aligned}$	$C_L = 15pF$ $C_L = 50pF$		4.0 6.5	5.6 9.1	1.0 1.0	7.5 11.0	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time OE to O	$V_{CC} = 2.7V$ $R_L = 1k\Omega$	C <sub>L</sub> = 50pF		10.0	15.7	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$	C <sub>L</sub> = 50pF		8.3	11.2	1.0	13.0	
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7V$ $V_{CC} = 3.3 \pm 0.3V$	$C_L = 50pF$ $C_L = 50pF$			1.5 1.5		1.5 1.5	ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

## **CAPACITIVE CHARACTERISTICS**

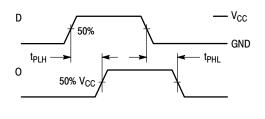
		T <sub>A</sub> = 25°C		T <sub>A</sub> = −40 to 85°C			
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
Cin	Input Capacitance		4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)		14				pF

<sup>2.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per bit). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## $\textbf{NOISE CHARACTERISTICS} \text{ (Input } t_{r} = t_{f} = 3.0 \text{ns}, \ C_{L} = 50 \text{pF}, \ V_{CC} = 3.3 \text{V}, \ Measured in SOIC Package)}$

		T <sub>A</sub> = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.5	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

## **SWITCHING WAVEFORMS**



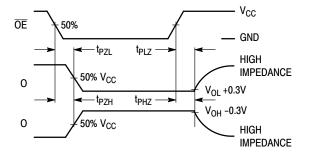
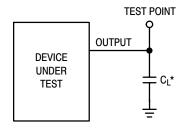
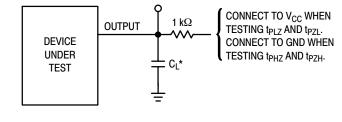


Figure 2.

Figure 3.

## **TEST CIRCUITS**





TEST POINT

\*Includes all probe and jig capacitance

Figure 4. Propagation Delay Test Circuit

Figure 5. Three-State Test Circuit

## **ORDERING INFORMATION**

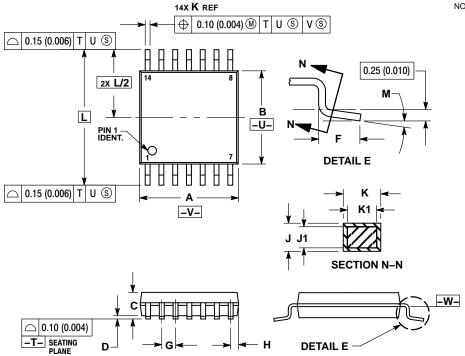
Device	Package	Shipping <sup>†</sup>
MC74LVX125DG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74LVX125DR2G	SOIC-14 NB (Pb-Free)	2500 Tape & Reel
MC74LVX125DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LVX125DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>Includes all probe and jig capacitance

### PACKAGE DIMENSIONS

## TSSOP-14 CASE 948G **ISSUE B**



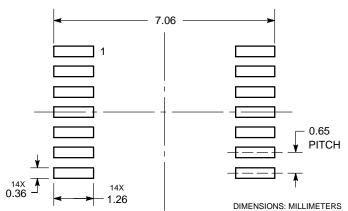
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER

  - 1. DIMENSIONING AND TOLERANCING PER
    ANSI Y14.5M, 1982.
    2. CONTROLLING DIMENSION: MILLIMETER.
    3. DIMENSION A DOES NOT INCLUDE MOLD
    FLASH, PROTRUSIONS OR GATE BURRS.
    MOLD FLASH OR GATE BURRS SHALL NOT
    EXCEED 0.15 (0.006) PER SIDE.
    4. DIMENSION B DOES NOT INCLUDE
    INTERLEAD FLASH OR PROTRUSION.
    INTERLEAD FLASH OR PROTRUSION SHALL
    NOT EXCEED 0.25 (0.010) PER SIDE.
    5. DIMENSION K DOES NOT INCLUDE DAMBAR
    PROTRUSION. ALLOWABLE DAMBAR
    PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
    EXCESS OF THE K DIMENSION AT MAXIMUM
    MATERIAL CONDITION.
    6. TERMINAL NUMBERS ARE SHOWN FOR
    REFERENCE ONLY.
    7. DIMENSION A AND B ARE TO BE
    DETERMINED AT DATUM PLANE -W-.

    MILLIMETERS INCHES

	MILLIN	IETERS	RS INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007 0.010	
L	6.40 BSC		0.252	BSC
М	0 °	8 °	0°	8 °

## **SOLDERING FOOTPRINT\***

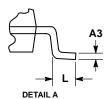


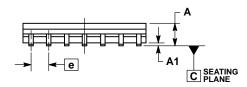
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

# SOIC-14 NB CASE 751A-03 ISSUE K В

0.25 M C A S B S

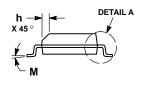




13X **b** 

Н

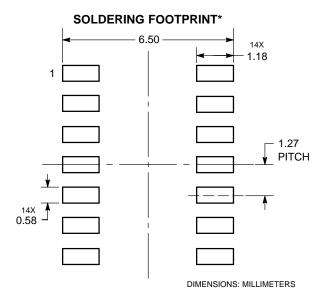
⊕ 0.25 M B M



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27	BSC	0.050	BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7°



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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