# **Quad 2-Input NOR Gate**

The MC74VHC02 is an advanced high speed CMOS 2-input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### **Features**

- High Speed:  $t_{PD} = 3.6 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V<sub>OLP</sub> = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

- Chip Complexity: 40 FETs or 10 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

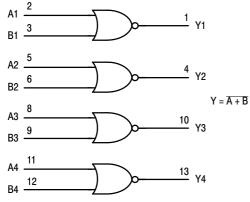


Figure 1. LOGIC DIAGRAM

1



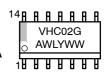
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**MARKING DIAGRAMS** 



SOIC-14 **D SUFFIX CASE 751A** 





TSSOP-14 **DT SUFFIX CASE 948G** 

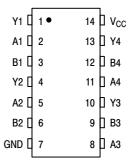


= Assembly Location

WL, L = Wafer Lot = Year = Work Week G or - Pb-Free Package

(Note: Microdot may be in either location)

#### **PIN ASSIGNMENT**



# **FUNCTION TABLE**

Inp	Inputs		
Α	В	Υ	
L	L	Н	
L	Н	L	
Н	L	L	
Н	Н	L	

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

#### **MAXIMUM RATINGS**

Symbol	Parameter	r	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage		- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage		- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current		- 20	mA
I <sub>OK</sub>	Output Diode Current		± 20	mA
l <sub>out</sub>	DC Output Current, per Pin		± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GI	ND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature		- 65 to + 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	V	/lin	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2	2.0	5.5	V
V <sub>in</sub>	DC Input Voltage		0	5.5	V
V <sub>out</sub>	DC Output Voltage		0	$V_{CC}$	V
T <sub>A</sub>	Operating Temperature	-	40	+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $V_{CC} = 3.3^{\circ}$ $V_{CC} = 5.0^{\circ}$		0	100 20	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>	1	Γ <sub>A</sub> = 25°	С	$T_{A} = -40$	0 to 85°C	
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> x 0.7			1.50 V <sub>CC</sub> x 0.7		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> x 0.3		0.50 V <sub>CC</sub> x 0.3	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4\text{mA}$ $I_{OL} = 8\text{mA}$	3.0 4.5			0.36 0.36		0.44 0.44	
l <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μА
I <sub>CC</sub>	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	μΑ

# AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$ )

					T <sub>A</sub> = 25°C		T <sub>A</sub> = - 40	) to 85°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y	$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		5.6 8.1	7.9 11.4	1.0 1.0	9.5 13.0	ns
		$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15pF$ $C_L = 50pF$		3.6 5.1	5.5 7.5	1.0 1.0	6.5 8.5	
C <sub>in</sub>	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0V		Ī
$C_{PD}$	Power Dissipation Capacitance (Note 1)	15	pF	

<sup>1.</sup> CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per gate).  $C_{PD}$  is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

# **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

		T <sub>A</sub> =	25°C	
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	- 0.3	- 0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.5	V

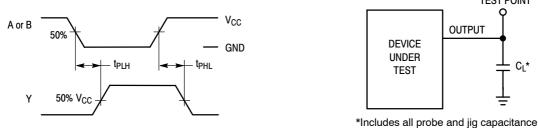


Figure 2. Switching Waveforms

Figure 3. Test Circuit

**TEST POINT** 

 $C_L^*$ 

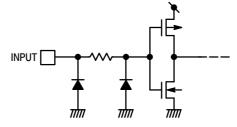


Figure 4. Input Equivalent Circuit

# **ORDERING INFORMATION**

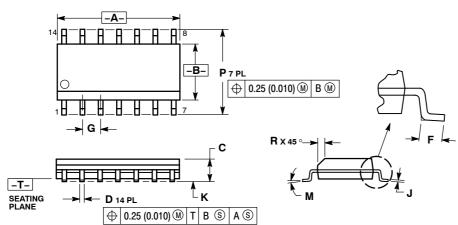
Device	Package	Shipping <sup>†</sup>
MC74VHC02DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHC02DTR2G	TSSOP-14*	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>This package is inherently Pb-Free.

# **PACKAGE DIMENSIONS**

# SOIC-14 CASE 751A-03 **ISSUE J**



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

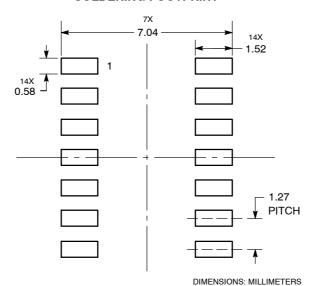
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

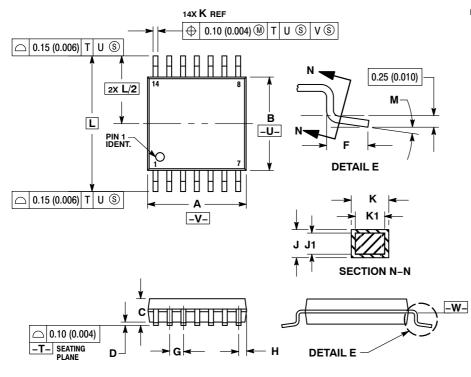
	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

# **SOLDERING FOOTPRINT**



#### PACKAGE DIMENSIONS

# TSSOP-14 CASE 948G-01 ISSUE B



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI Y14.5M, 1982.

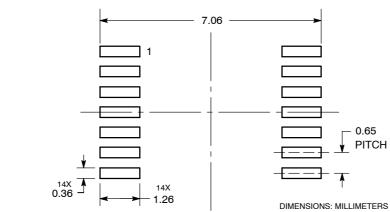
  CONTROLLING DIMENSION: MILLIMETER.

  DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  DIMENSION B DOES NOT INCLUDE
- DIMENSION B DOES NOT INCLUDE
  INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL
  NOT EXCEED 0.25 (0.101) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
Κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0 °	8 °	0 °	8 °	

#### SOLDERING FOOTPRINT



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