

UNIVERSAL
4-BIT SHIFT REGISTER

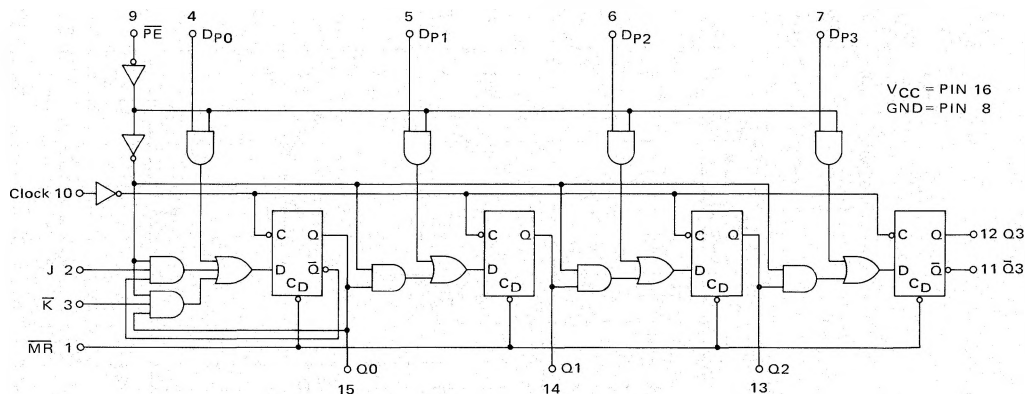
MC9300/MC8300 series

MC9300L*
MC8300L,P*

Input Loading Factor
J, $\bar{K}$, MR, D_{P0}, D_{P1}, D_{P2}, D_{P3} = 1
PE = 2.3
Clock = 4
Output Loading Factor = 6
Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 25 ns typ

This serial/parallel shift register consists of four flip-flops operated in the synchronous mode. Functions available are shift left, shift right, serial-to-serial, parallel-to-parallel, serial-to-parallel, and parallel-to-serial conversion.

This device operates on the positive-going edge of the clock pulse in both the serial and parallel mode. The device includes an internal clock buffer, input clamp diodes to reduce ringing, Q outputs for all four stages, $\bar{Q}$ output for the last stage, synchronous parallel entry, and an asynchronous master reset. The J and $\bar{K}$ inputs are available, and may be tied together to produce a D input.



INPUT and OUTPUT LOADING FACTORS
with respect to MTL and MDTL families

FAMILY	MC9300 INPUT LOADING FACTOR	MC9300 OUTPUT LOADING FACTOR
MC9300	1.0	6
MC500	1.06	6.4
MC2100	0.7	4.25
MC3100	0.7	3.6
MC4300	1.0	4.65
MC5400	1.0	4.65
MC9300**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	5.6

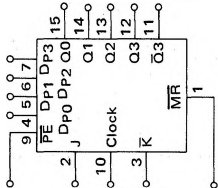
FAMILY	MC8300 INPUT LOADING FACTOR	MC8300 OUTPUT LOADING FACTOR
MC8300	1.0	6
MC400	1.0	5.45
MC2000	0.6	4.5
MC3000	0.7	4.25
MC4000	1.0	5.3
MC7400	1.0	5.3
MC8300**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	6.1

**Due to logic "1" state drive limitations of the MDTL family.

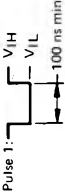
*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one parallel data input. Other parallel data inputs are tested in the same manner. Further, test procedures are shown for only one output. Complete testing according to the Functional Test Diagram.

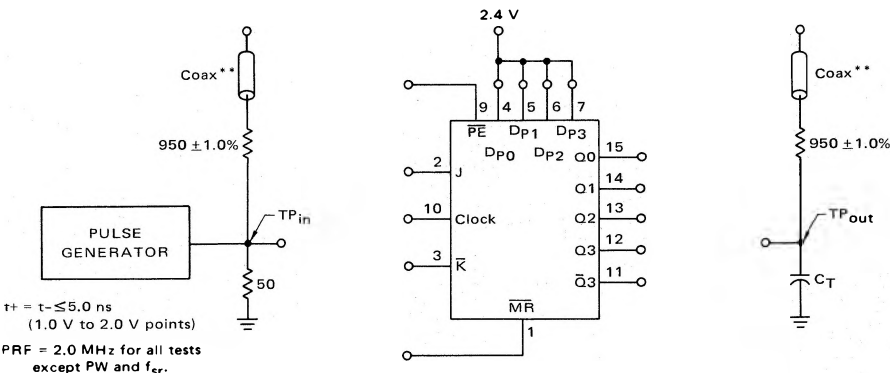


Characteristic		Pin Under Test	MC9300 Test Limits												MC8300 Test Limits												TEST CURRENT/VOLTAGE VALUE												Pulse 1		Gnd																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
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MC9300, MC8300 (continued)

SWITCHING TIME TEST CIRCUIT



$t^+ = t^- \leq 5.0$ ns
(1.0 V to 2.0 V points)
PRF = 2.0 MHz for all tests
except PW and f_{sr} .

Three pulse generators are
required and must be slaved
together to provide the wave-
forms shown.

** The coax delays from input to scope and output to scope must be matched. The
scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the
scope termination impedance constitute a 20:1 attenuator probe. Coax shall be
CT-070-50 or equivalent.

$C_T = 15$ pF = total parasitic capacitance, which includes probe and wiring
capacitances.

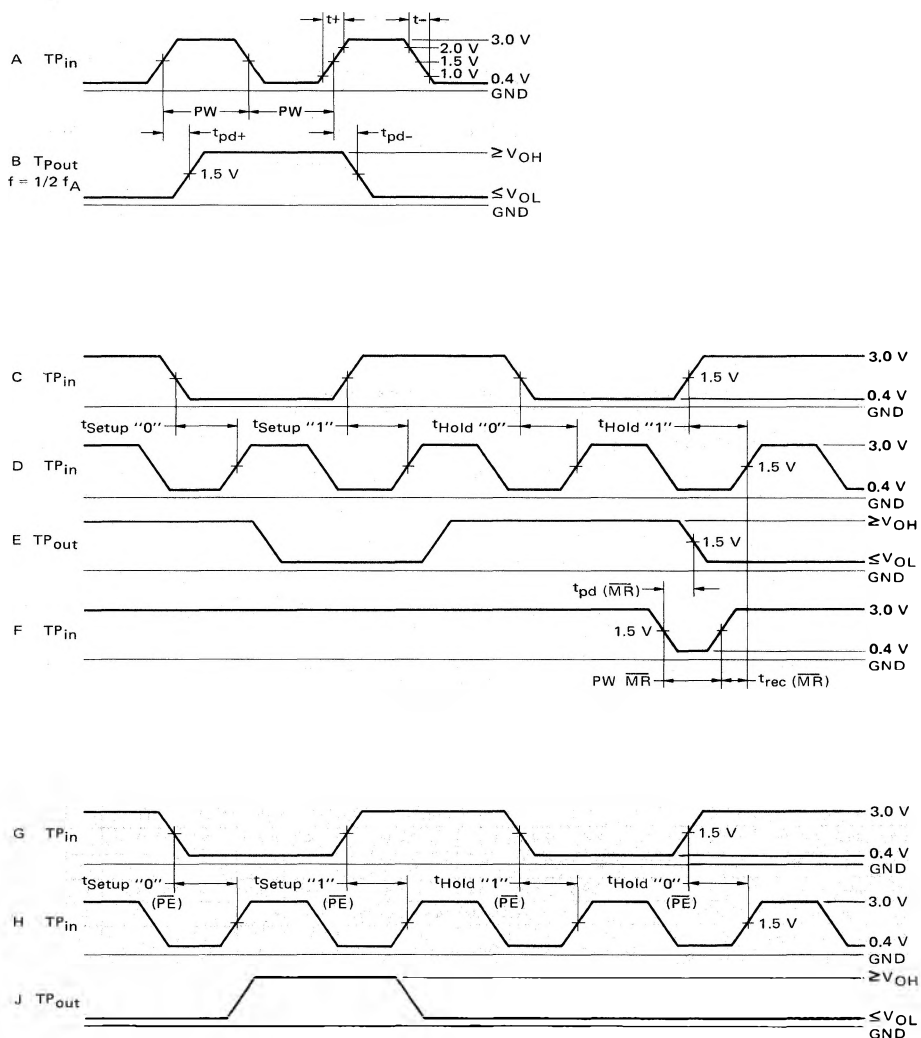
SWITCHING TIME TEST PROCEDURES ($T_A = 25^\circ\text{C}$)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST	INPUT								OUTPUT Pin 12 Q3	VALUE			
			Pin 1 MR	Pin 2 J	Pin 3 K	Pins 4, 5, 6 Dp0, Dp1, Dp2	Pin 7 Dp3	Pin 9 PE	Pin 10 Clock	Min		Typ	Max	Unit	
Turn-Off Delay, Clock to Q3	t _{pd+}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	—	18	35	ns	
Turn-On Delay, Clock to Q3	t _{pd-}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	—	25	45	ns	
Maximum Shift Rate	f _{sr}	12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	15	25	—	MHz	
Minimum Clock Pulse Width	PW	Tested during each of the above tests.									—	13	35	ns	
Minimum Data Input Setup Time (Serial or Parallel Inputs)	t _{Setup} “1” t _{Setup} “0”	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ①	—	14	35	ns	
Maximum Data Input Hold Time (Serial or Parallel Inputs)	t _{Hold} “1” t _{Hold} “0”	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ②	0	16	—	ns	
Minimum Recovery Time, MR Input	t _{rec}	Tested during Data Input t _{Setup} and t _{Hold} tests.									—	19	30	ns	
Minimum MR Pulse Width	PW	Tested during Data Input t _{Setup} and t _{Hold} tests.									—	15	30	ns	
Turn-On Delay, MR to Q3	t _{pd-}	1,12	F	2.4 V	Gnd	2.4 V	2.4 V	Gnd	D	E	—	29	45	ns	
Minimum PE Input Setup Time	t _{Setup} “1” t _{Setup} “0”	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ①	—	22	45	ns	
Maximum PE Input Hold Time	t _{Hold} “1” t _{Hold} “0”	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ②	10	18	—	ns	

① Output toggles. ② Output does not toggle.

MC9300, MC8300 (continued)

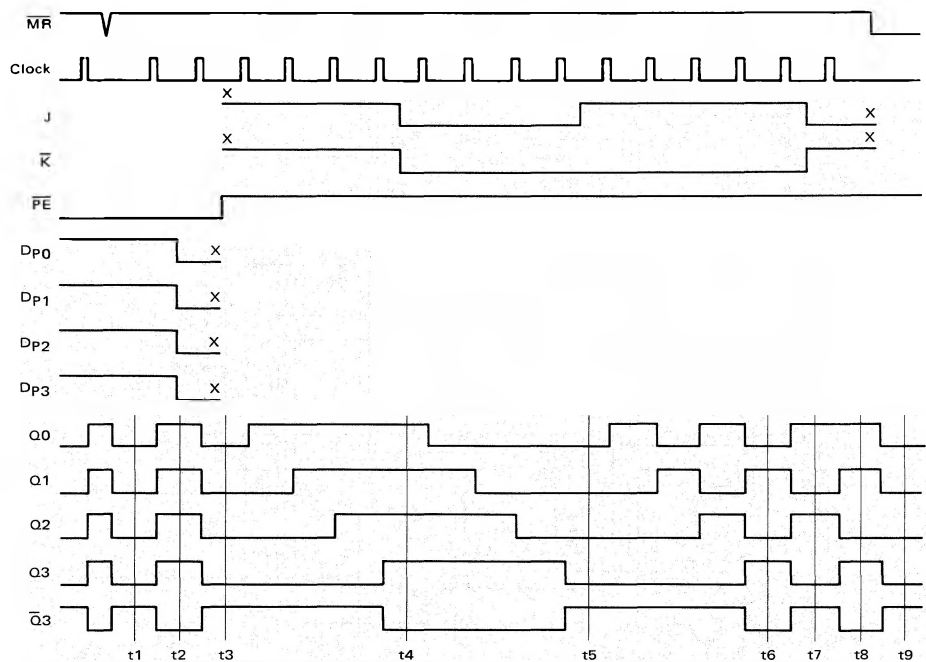
VOLTAGE WAVEFORMS



FUNCTIONAL DESCRIPTION

1. J and $\bar{K}$ inputs are made available on the first flip-flop of the register to provide full input logic capability without restrictions other than setup and release times. The simpler D type input can be obtained by wiring the J and $\bar{K}$ inputs together.
2. Parallel data inputs are provided to each stage of the register. These inputs are enabled only when the Parallel Enable is low. Information is transferred to the register on the positive transition of the clock. This information is shifted to the right on the next positive transition of the clock if the Parallel Enable is high. Shift left operation is achieved by driving the parallel inputs with the Q outputs of the right-adjacent stage. For this operation the Parallel Enable must be low.
3. An internal clock buffer has been included to reduce clock input loading, allowing the clock input of the register to be driven by a single gate.
4. The true output is provided for all stages; the complementary output is also provided for the last stage.
5. The master asynchronous reset input will clear the register independent of the conditions of the other inputs.

FUNCTIONAL DIAGRAM



X = Voltage level of unspecified area(s) preceding or following "X" are unimportant.

CIRCUIT SCHEMATIC

