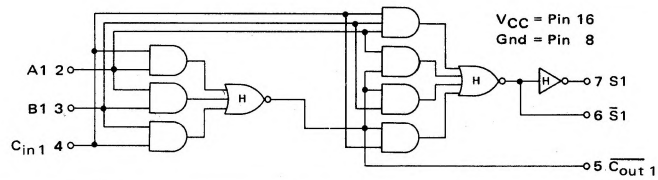
MC9304L*
MC8304L,P*

ADDER 1

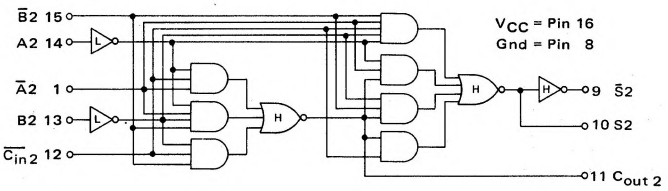
INPUT			OUTPUT		
C_{in1}	B1	A1	$\overline{C_{out1}}$	$\overline{S1}$	S1
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

This device consists of two independent, high-speed, binary full adders, with complementary Sum outputs. Adder two has provisions for both active high and active low inputs. Carry In and Carry Out of adder two are complementary to those of adder one. These choices provide greater design flexibility and minimum package count.



FULL ADDER 1

FULL ADDER 2



Input Loading Factors:
Adder 1: A1, B1, C_{in1} = 4
Adder 2: $\overline{A2}$, $\overline{B2}$, $\overline{C_{in2}}$ = 4
A2, B2 = 1

Output Loading Factors:
Adder 1: $\overline{C_{out1}}$ = 7
S1 = 10
$\overline{S1}$ = 9
Adder 2: C_{out2} = 7
S2 = 9
$\overline{S2}$ = 10

Total Power Dissipation = 110 mW typ/pkg

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	t_{pd-}		t_{pd+}	
	$\overline{C_{out}}$	$\overline{S}$	$\overline{C_{out}}$	$\overline{S}$
C_{in}	8.0	–	8.0	–
A1	–	25	–	28

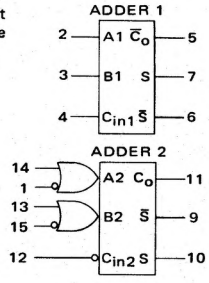
ADDER 2

INPUT					OUTPUT		
$\overline{C_{in}}$ 2	B2	A2	$\overline{B2}$	$\overline{A2}$	C_{out} 2	S2	$\overline{S2}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

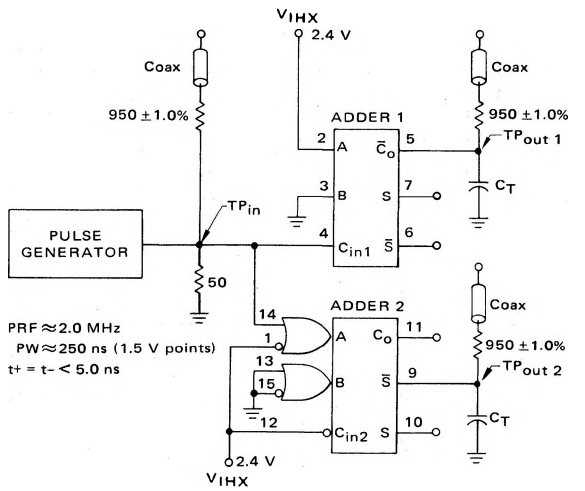
Test procedures are shown for only one adder. The other adder is tested in the same manner. Output tests are shown for only one set of input conditions. To complete testing, sequence through all input combinations according to the appropriate truth table.

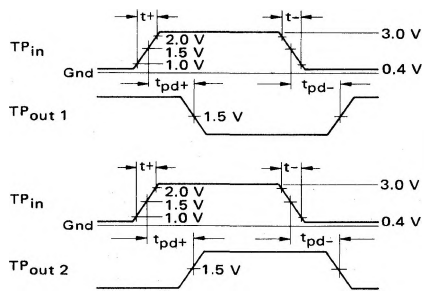


@ Test Temperature		TEST CURRENT / VOLTAGE VALUES																		
		mA										Volts								
		I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OL5}	I_{OL6}	I_{OH1}	I_{OH2}	I_{OH3}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC9304	−55°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-	0.85	2.0	0.40	4.5	5.0	4.5	5.5	5.5	-
	+25°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-10	0.85	1.7	0.40	4.5	5.0	4.5	5.5	2.4	
	+125°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-	0.85	1.4	0.40	4.5	5.0	4.5	5.5	-	
MC8304	0°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-	0.8	1.9	0.45	4.5	5.0	4.75	5.25	-	
	+25°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-10	0.9	1.8	0.45	4.5	5.0	4.75	5.25	2.4	
	+75°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-	0.8	1.6	0.45	4.5	5.0	4.75	5.25	-	

Characteristic	Symbol	Pin Under Test	MC9304 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC8304 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OL5}	I_{OL6}	I_{OH1}	I_{OH2}	I_{OH3}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																																	
Forward Current	I_{F1}	1	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1	2,3,4,12,13,14,15	-	-	16	-	8
		12	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4		-	-	-	-	-	-	-	-	-	-	-	-	12	1,2,3,4,13,14,15	-	-		-	
		13	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	-	-	-	-	-	-	-	13	1,2,3,4,12,14,15	-	-		-	
		14	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,12,13,15	-	-		-	
		15	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4		-	-	-	-	-	-	-	-	-	-	-	-	15	1,2,3,4,12,13,14	-	-		-	
	I_{F2}	1	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1	2,3,4,12,13,14,15	-	16	-	-	8
		12	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64		-	-	-	-	-	-	-	-	-	-	-	-	12	1,2,3,4,13,14,15	-	-		-	
		13	-	-1.24	-	-1.24	-	-1.24	-	-1.41	-	-1.41	-	-1.41		-	-	-	-	-	-	-	-	-	-	-	-	13	1,2,3,4,12,14,15	-	-		-	
		14	-	-1.24	-	-1.24	-	-1.24	-	-1.41	-	-1.41	-	-1.41		-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,12,13,15	-	-		-	
		15	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64		-	-	-	-	-	-	-	-	-	-	-	-	15	1,2,3,4,12,13,14	-	-		-	
Leakage Current	I_R	1	-	240	-	240	-	240	-	240	-	240	-	240	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	16	-	2,3,4,8,12,13,14,15
		12	-	240	-	240	-	240	-	240	-	240	-	240		-	-	-	-	-	-	-	-	-	-	-	-	-	12	-	-		-	1,2,3,4,8,13,14,15
		13	-	60	-	60	-	60	-	60	-	60	-	60		-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-		-	1,2,3,4,8,12,14,15
		14	-	60	-	60	-	60	-	60	-	60	-	60		-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-		-	1,2,3,4,8,12,13,15
		15	-	240	-	240	-	240	-	240	-	240	-	240		-	-	-	-	-	-	-	-	-	-	-	-	-	15	-	-		-	1,2,3,4,8,12,13,14
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	16	-	8
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	12	-	-	-	-	-	-		-	
		13	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	13	-	-	-	-	-	-		-	
		14	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	-		-	
		15	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	15	-	-	-	-	-	-		-	
Output																																	
Output Voltage	V_{OL}	9	-	0.4	-	0.4	-	0.4	-	0.45	-	0.45	-	0.45	Vdc	9	-	-	-	-	-	-	-	-	-	1,12,13,14,15	-	-	-	-	-	16	-	8
		10	-		-		-		-		-		-			-	10	-	-	-	-	-	-	-	12,13,14,15	1	-	-	-	-		-	
		11	-		-		-		-		-		-			-	-	11	-	-	-	-	-	-	12,13,14	1,15	-	-	-	-		-	
		9	-		-		-		-		-		-			-	-	-	9	-	-	-	-	-	1,12,13,14,15	-	-	-	-	16		-	
		10	-		-		-		-		-		-			-	-	-	-	10	-	-	-	-	12,13,14,15	1	-	-	-			-	
		11	-		-		-		-		-		-			-	-	-	-	-	11	-	-	-	12,13,14	1,15	-	-	-			-	
	V_{OH}	9	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	-	-	-	-	-	9	-	-	-	12,13,14,15	1	-	-	-	-	16	-	8
		10		-		-		-		-		-		-		-	-	-	-	-	-	-	10	-	-	1,12,13,14,15	-	-	-	-			-	
		11		-		-		-		-		-		-		-	-	-	-	-	-	-	-	11	-	1,12,13,14,15	-	-	-	-			-	
Power Requirements (Total Device)																																	
Power Supply Drain	I_{PD}	16	-	-	-	45	-	-	-	-	-	50	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	16	-	-	8
Switching Parameters																Pulse In		Pulse Out																
Turn-On Delay	t_{pd-1}	4/5	-	-	-	13	-	-	-	-	-	15	-	-	ns	4		5		-	-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
	t_{pd-2}	14/9	-	-	-	35	-	-	-	-	-	40	-	-	ns	14		9		-	-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
Turn-Off Delay	t_{pd+1}	4/5	-	-	-	13	-	-	-	-	-	15	-	-	ns	4		5		-	-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
	t_{pd+2}	14/9	-	-	-	40	-	-	-	-	-	45	-	-	ns	14		9		-	-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

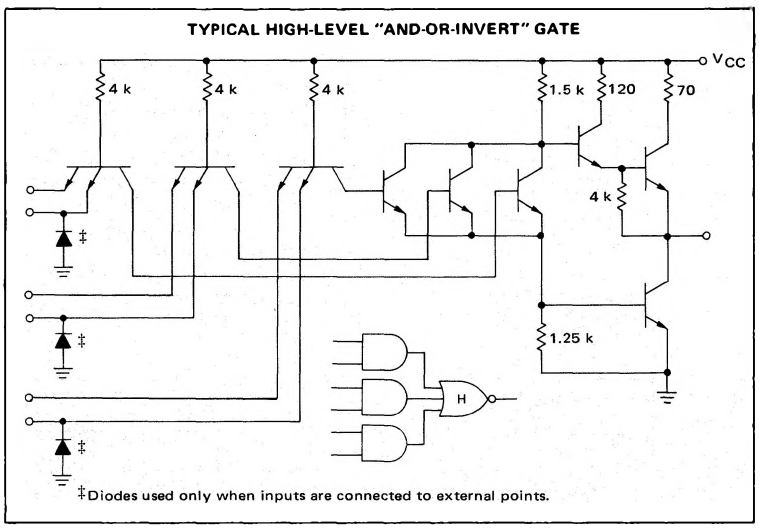


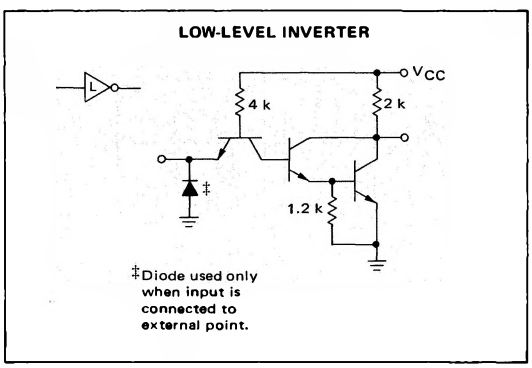


The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

This full adder is constructed using high and low level gates interconnected as shown by the logic diagram.





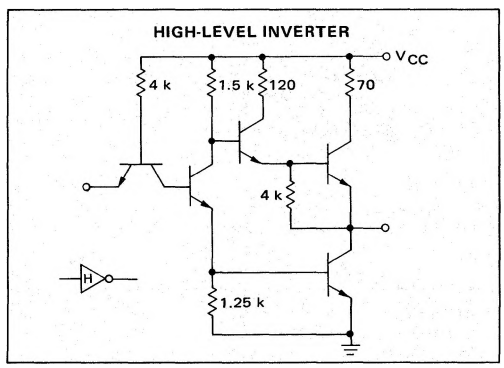


FIGURE 1 – FUNCTION BLOCK DIAGRAM

This diagram illustrates the adder function of the MC9304/8304 using either active low or high inputs.