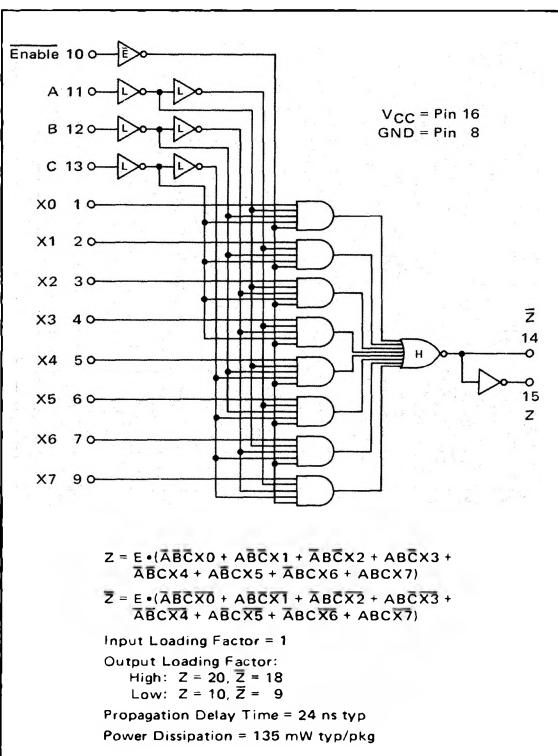


8-CHANNEL
DATA SELECTOR

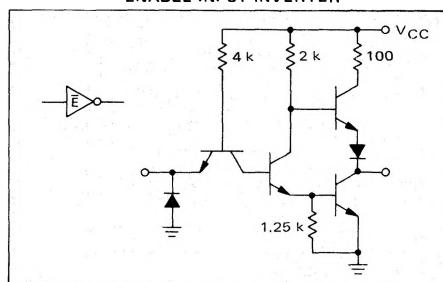
MC9300/MC8300 series

MC9312L*
MC8312L,P*

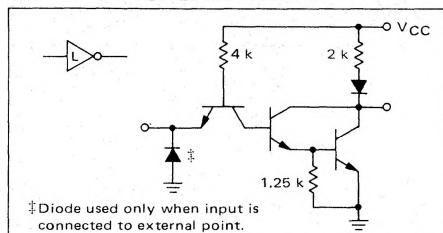


This 8-channel data selector is constructed from high-level and low-level gates interconnected as shown in the logic diagram. It is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of the select inputs, A, B, and C. Complementary outputs are provided. The Enable input is active in the low state. When the Enable input is high, the \bar{Z} output is high and the Z output low, regardless of the state of the other inputs.

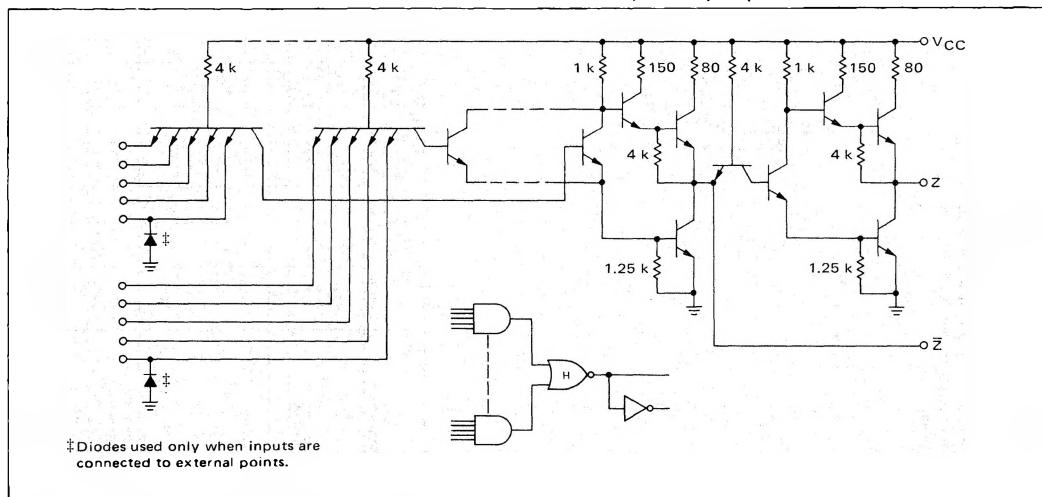
ENABLE-INPUT INVERTER



LOW-LEVEL INVERTER



HIGH-LEVEL "AND-OR-INVERT" GATE (Complementary Outputs)

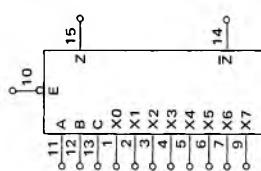


* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

MC9312, MC8312 (continued)

TRUTH TABLE

$p = \text{Input level}$ does not affect output.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table. Additionally, test all input-output combinations according to the truth table.

TEST CURRENT/VOLTAGE VALUES							
	I _{H1}	I _{H2}	V _{IL}	V _{IH}	V _F	V _R	
1.1	-0.06	-	0.80	2.0	0.4	-	
1.2	-1.06	-1.0	0.90	1.7	0.4	4.5	
1.3	-1.12	-1.0	-	0.80	1.4	0.4	4.5
1.4	-1.12	-1.08	-	0.85	1.9	0.45	-
1.5	-1.12	-1.08	-10	0.85	1.8	0.45	4.5

TEST CURRENT/VOLTAGE VALUES															
		Volts													
		mA							mA						
@ Test Temperature		I_{OL1}	I_{OL2}	I_{OL3}	$ I_{OL4} $	$ I_{OH1} $	$ I_{OH2} $	$ I_D $	V_{IL}	V_{IH}	V_F	V_C	V_{CL}	V_{CCH}	V_{HX}
MC9312	-55°C	11.2	12.4	14.4	16.0	-1.2	-1.08	-	0.80	2.0	0.4	4.5	5.5	-	-
	+25°C	11.2	12.4	14.4	16.0	-1.2	-1.08	-10	0.90	1.7	0.4	4.5	5.5	2.4	-
MC8312	-55°C	11.2	12.4	14.4	16.0	-1.2	-1.08	-	0.80	1.4	0.4	4.5	5.5	-	-
	+25°C	12.7	14.1	14.4	16.0	-1.2	-1.08	-	0.85	1.9	0.45	5.0	4.75	5.25	-
MC9312 Test Limits		12.7	14.1	14.4	16.0	-1.2	-1.08	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
MC9312 Test Limits		12.7	14.1	14.4	16.0	-1.2	-1.08	-	0.85	1.6	0.45	4.5	5.0	4.75	5.25
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:															
Characteristic		Pin	Under Test	-55°C	+25°C	+125°C	0°C	+25°C	0°C	Min	Max	Min	Max	Min	Max
Input Forward Current		I _{F1}	1	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6
Lakage Current		I _H	1	-	-1.24	-	-1.24	-	-1.41	-	-1.41	-	-1.41	-	-1.41
Clamp Voltage		V _D	1	-	-	-15	-	-	-15	-	-15	-	-15	-	-15
Output Output Voltage		V _{O1}	14	-	0.4	-	0.4	-	0.45	-	0.45	-	0.45	-	0.45
Power Requirements (Total Device)		V _{O2}	14	-	0.4	-	0.4	-	0.45	-	0.45	-	0.45	-	0.45
Power Supply Drain		V _{OR}	14	-	0.4	-	0.4	-	0.45	-	0.45	-	0.45	-	0.45
Switching Parameters		I _{PDH}	16	-	40	-	40	-	43	-	43	mADC	-	-	-
Turn-On Delay		I _{pd+}	11/15	-	-	-	-	-	-	36	-	-	-	-	-
Turn-Off Delay		I _{pd-}	11/15	-	-	-	-	-	-	34	-	-	-	-	-

MC9312, MC8312 (continued)

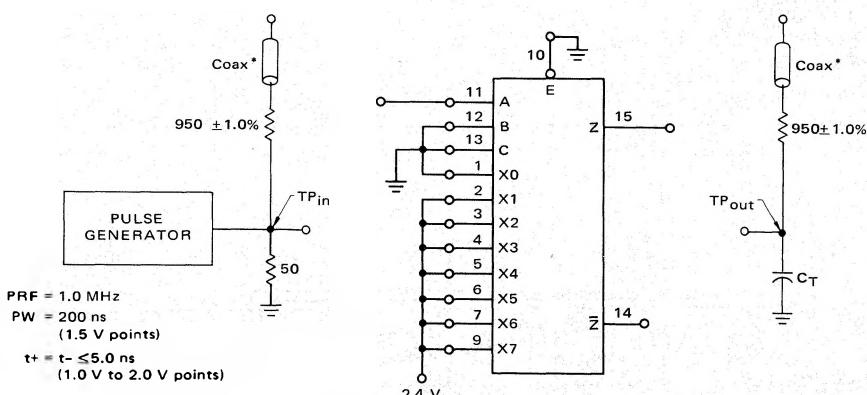
**INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families**

FAMILY	MC9312 INPUT LOADING FACTOR	MC9312 OUTPUT LOADING FACTOR	
		Z	\bar{Z}
MC9300	1.0	10	9.0
MC500	1.06	10.6	9.5
MC2100	0.7	7.0	6.3
MC3100	0.7	7.0	6.3
MC4300	1.0	10	9.0
MC5400	1.0	7.75	7.0
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	9.4	8.4

FAMILY	MC8312 INPUT LOADING FACTOR	MC8312 OUTPUT LOADING FACTOR	
		Z	\bar{Z}
MC8300	1.0	10	9.0
MC400	1.0	9.0	8.1
MC2000	0.6	6.0	5.4
MC3000	0.7	7.4	6.6
MC4000	1.0	10	9.0
MC7400	1.0	8.75	7.8
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	10.8	9.7

* Due to logic "1" state drive limitations of the MDTL family.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe and wiring capacitances.

