PRESETTABLE
4-BIT BINARY COUNTER

MC9316L*
MC8316L,P*

The MC9316/8316 hexadecimal counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

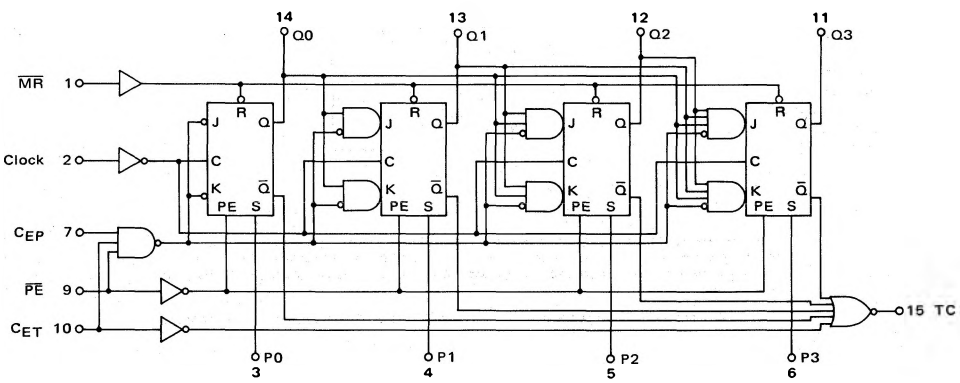
Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

COUNT SEQUENCE TRUTH TABLE

	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Input Loading Factors:
$\overline{MR}$, C_{EP} = 1
Clock, $\overline{PE}$, C_{ET} = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 14 to 35 ns typ
Toggle Frequency = 28 MHz typ

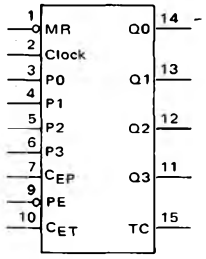


V_{CC} = Pin 16
GND = Pin 8

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

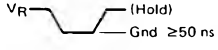
Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table.



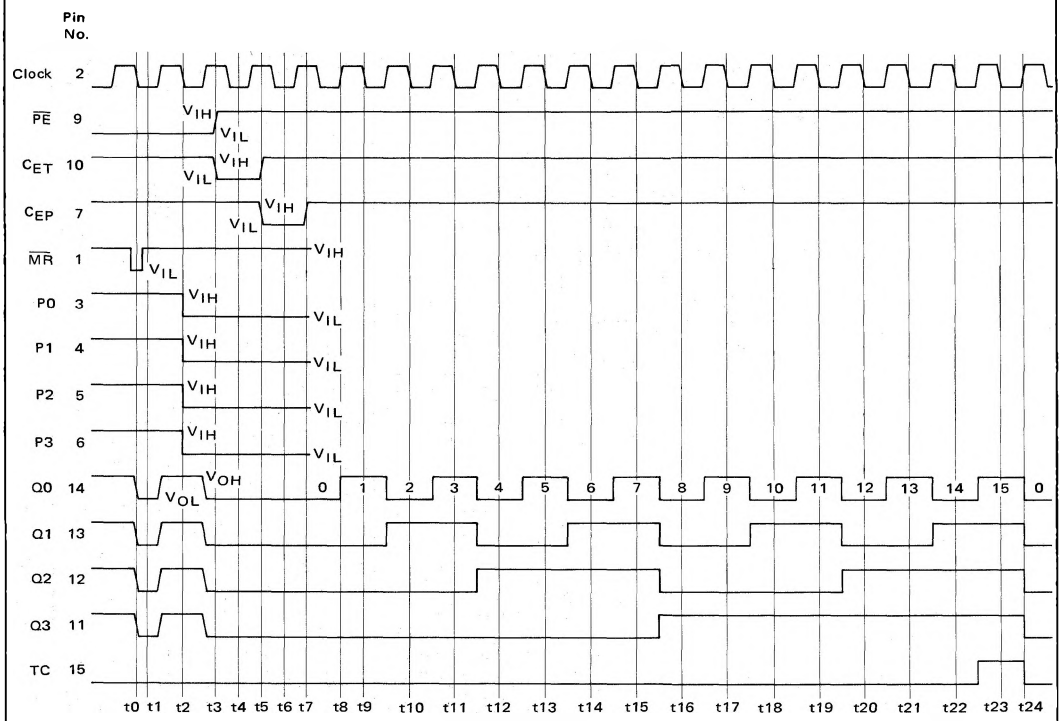
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9316	-55°C	9.6	7.44	-0.36	–	0.80	2.0	0.4	4.6	5.0	4.5	5.5
	+25°C	9.6	7.44	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
	+125°C	9.6	7.44	-0.36	–	0.80	1.4	0.4	4.5	5.0	4.5	5.5
MC8316	0°C	9.6	8.50	-0.36	–	0.85	1.9	0.45	4.5	5.0	4.75	5.25
	+25°C	9.6	8.50	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
	+75°C	9.6	8.50	-0.36	–	0.85	1.6	0.45	4.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9316 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8316 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	8
		2	–	-3.2	–	-3.2	–	-3.2	mAdc	–	-3.2	–	-3.2	–	-3.2	mAdc	–	–	–	–	–	–	2	–	–	–	16	8
		3	–	-1.07	–	-1.07	–	-1.07	mAdc	–	-1.07	–	-1.07	–	-1.07	mAdc	–	–	–	–	–	–	3	–	–	–	16	8
Leakage Current	I_R	1	–	60	–	60	–	60	μAdc	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	1	–	–	16	8
		2	–	120	–	120	–	120	μAdc	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	2	–	–	16	8
		3	–	40	–	40	–	40	μAdc	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	–	3	–	–	16	8
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	16	–	–	8
Output																												
Output Voltage	V_{OL1}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	11	–	–	See Timing Diagram @ t1					–	16	8
	V_{OL2}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t4					16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t9					16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t10					16	–	8
	V_{OH}	11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t2					16	–	8
		11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t16					16	–	8
Power Requirements (Total Device) Power Supply Drain Current	I_{PD}	16	–	–	–	75	–	–	mAdc	–	–	–	75	–	–	mAdc	–	–	–	–	–	2,7 9,10	–	1*	16	–	–	8
Switching Parameters																	Pulse In		Pulse Out		V_{IHX} = 3.0 Vdc							
Turn-On Delay – Q	t_{pd-}	2,14	–	–	–	30	–	–	ns	–	–	–	30	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – Q	t_{pd+}	2,14	–	–	–	35	–	–	ns	–	–	–	35	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-On Delay – TC	t_{pd-}	2,15	–	–	–	40	–	–	ns	–	–	–	40	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – TC	t_{pd+}	2,15	–	–	–	60	–	–	ns	–	–	–	60	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8

*Apply after potentials have been applied to other pins.



TIMING DIAGRAM



NOTES

1. The Clock pulse must be in the high state during the high to low transition of C_{ET} and C_{EP}, and the low to high transition of $\overline{PE}$ for correct logic operation.
2. Pin conditions reflected on timing diagram for tests at time specified:

t0: Parallel (P) inputs high, Parallel Enable ($\overline{PE}$) low, asynchronous Master Reset ($\overline{MR}$) pulsed; Q outputs make transition from high to low.

t1: Measure both V_{OL1} and V_{OL2} on Q0, Q1, Q2, Q3 and TC before Clock goes high.

t2: Clock has been pulsed, Q outputs are high; measure V_{OH}.

t3: Clock is in high state while transitions of $\overline{PE}$ and C_{ET} occur (necessary condition). Parallel entry is now inhibited, P inputs are at the low level.

t4: Count enable (C_{ET}) is at the low level (disabled), count cannot occur; check Q outputs to see that they remain at the low level.

t5: C_{ET} is set to a high level and C_{EP} is set at the low level while the Clock is high.

t6: Check Q outputs to see that count is disabled, outputs remain low.

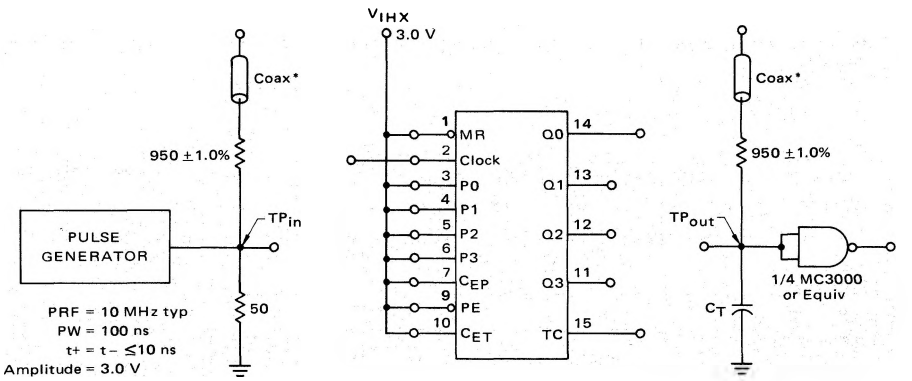
t7: C_{EP} is set high while Clock is high; count is now enabled.

t8: Clock is pulsed, count begins from 0000 to 0001.

t9 thru t23: Check Q and TC output states.

t24: Outputs go to low state, count begins (0000).

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.