

DUAL 8-BIT SHIFT REGISTER

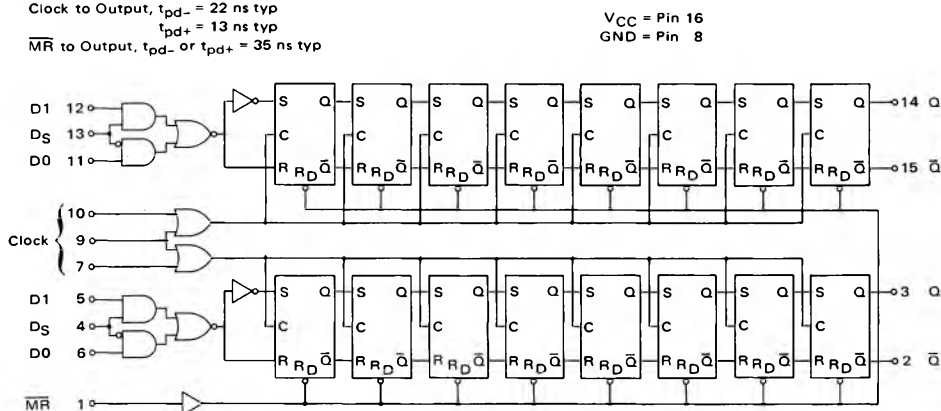
MC9300/MC8300 series

MC9328L* MC8328L,P*

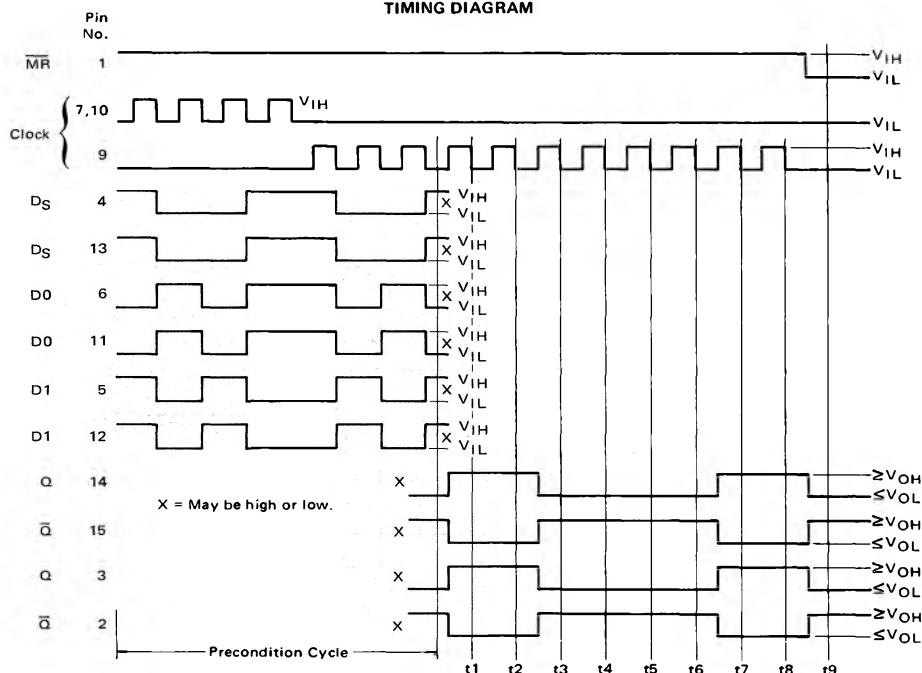
Input Loading Factors:
MR, D0, D1 = 1
D_S = 2
Clock - Pins 7, 10 = 1.5
Pin 9 = 3
Output Loading Factor = 6

Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = :
Clock to Output, t_{pd-} = 22 ns typ
t_{pd+} = 13 ns typ
MR to Output, t_{pd-} or t_{pd+} = 35 ns typ

The MC9328/8328 is a monolithic dual 8-bit serial shift register. Each 8-bit register is provided with a 2-input multiplexer circuit and complementary serial outputs. The two registers can be clocked together with a common line, or clocked separately with separate lines. A common Master Reset input is active in the low level and overrides all other inputs.



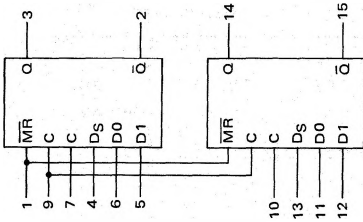
TIMING DIAGRAM



* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output of one half of the device. To complete testing, sequence through other inputs and outputs in the same manner



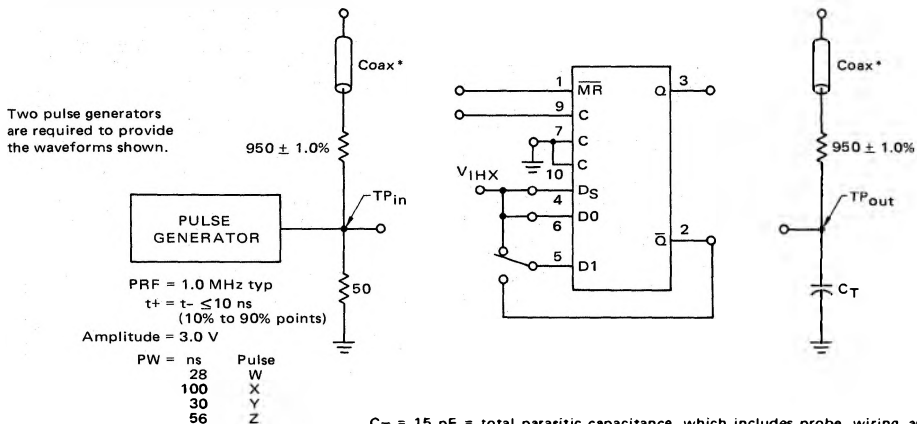
Characteristic		Pin Under Test	MC9328 Test Limits										MC8328 Test Limits										TEST CURRENT/VOLTAGE VALUES																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
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* Letters in parenthesis refer to waveform.

These pins tied together

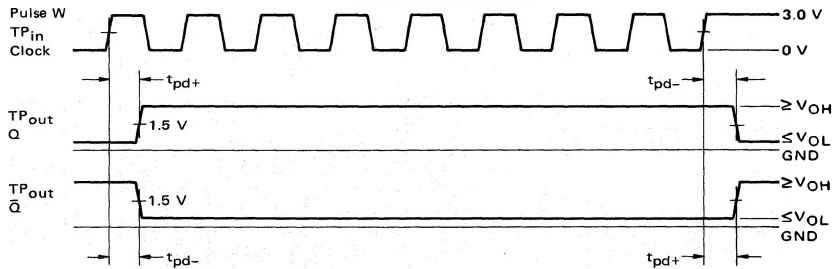
These pins tied together

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

CLOCK PROPAGATION DELAY



MASTER RESET PROPAGATION DELAY

