Product Brief

MC92701PB/D
Rev. 1, 11/2003

MC92701 BPON Layer Termination Device Product Brief

MOTOROLA intelligence everywhere™ | digital dna™

´This document provides a high-level description of the features and functions of the MC92701 broadband passive optical network (BPON) layer termination device. The MC92701 is compliant with ITU-T G.983 recommendations and is designed for use in optical network unit (ONU) and optical network termination (ONT) system applications. The MC92701 BPON layer termination device implements ITU-T G.983.4 dynamic bandwidth allocation (DBA), on-chip clock and data recovery (CDR), PON termination, and operations, administration, and maintenance (OAM) to provide a fully integrated solution with the Power QUICC communication processor for the ONU/ONT. The MC92701 BPON layer termination device has the capability of operating with one or two UTOPIA ports. This part is a standards-based solution for broadband access services for business enterprises and homes.

This document contains the following topics:

1 Overview

This section provides a high-level overview of the MC92701 key features.

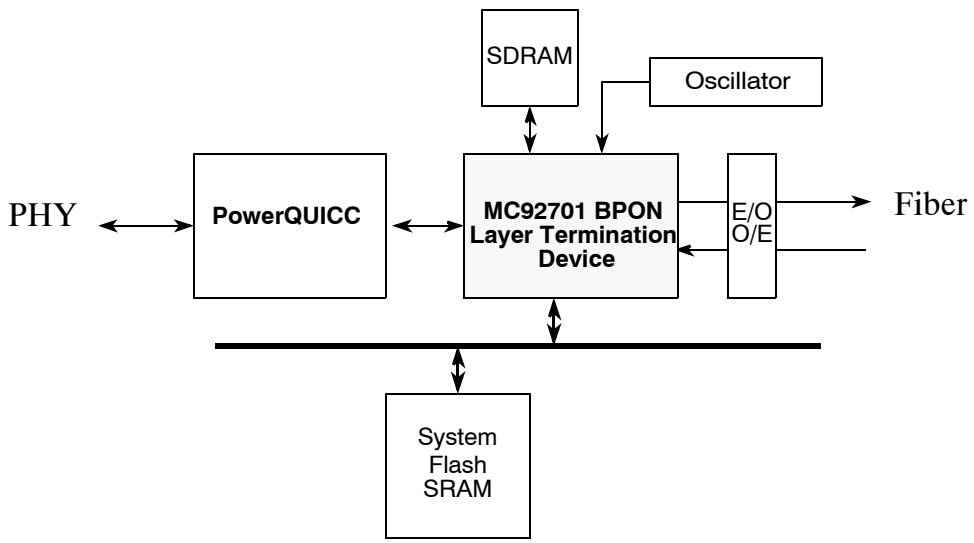
- Optical module interface clock and data recovery (CDR)—ITU-T G.983.1 compliant
- ITU-T G. 983.1-compliant
- Downstream 622/155 Mbps
- Upstream 155 Mbps

- Dynamic bandwidth assignment—ITU-T G.983.4 and ITU-T G.983.7-compliant
  - — Backward compatible with non-DBA OLT
  - — Supports status report (SR) and non-status report (NSR)
- Supports four classes of quality of service (QoS)
  - — Constant bit rate (CBR)
  - — Variable bit rate (VBR)
  - — Guaranteed frame rate (GFR)
  - — Unspecified bit rate (UBR)
- Supports all types of traffic containters (T-CONT) (1/2/3/4/5)
- Supports early packet discard (EPD) and partial packet discard (PPD)
- ATM cell processing with full OAM support
- Microprocessor unit (MPU) bus interface—PowerQUICC ^{TM} and PowerQUICC II^{TM}compatible
- Debugging and monitor features
- Supports two UTOPIA ports
- Design for test (JTAG IEEE 1149.1 compliant, full scan, full memory BIST)
- V_{DD} = 3.3V ± 0.3V 1.8V ± 0.15V
- 416 PBGA packages
- Operating temperature T_j from -40^{o} to +105^{o}C.

2 Feature Descriptions

2.1 Example of System Block Diagram

Figure 2-1 shows an application system block diagram.



E/O,O/E: Optical module (E/O:Upstream(Tx), O/E:Downstream(Rx))

Figure 2-1. System Block Diagram

2.2 MC92701 BPON Layer Termination Device Block Diagram

The MC92701 BPON layer termination device block diagram is shown in Figure 2.

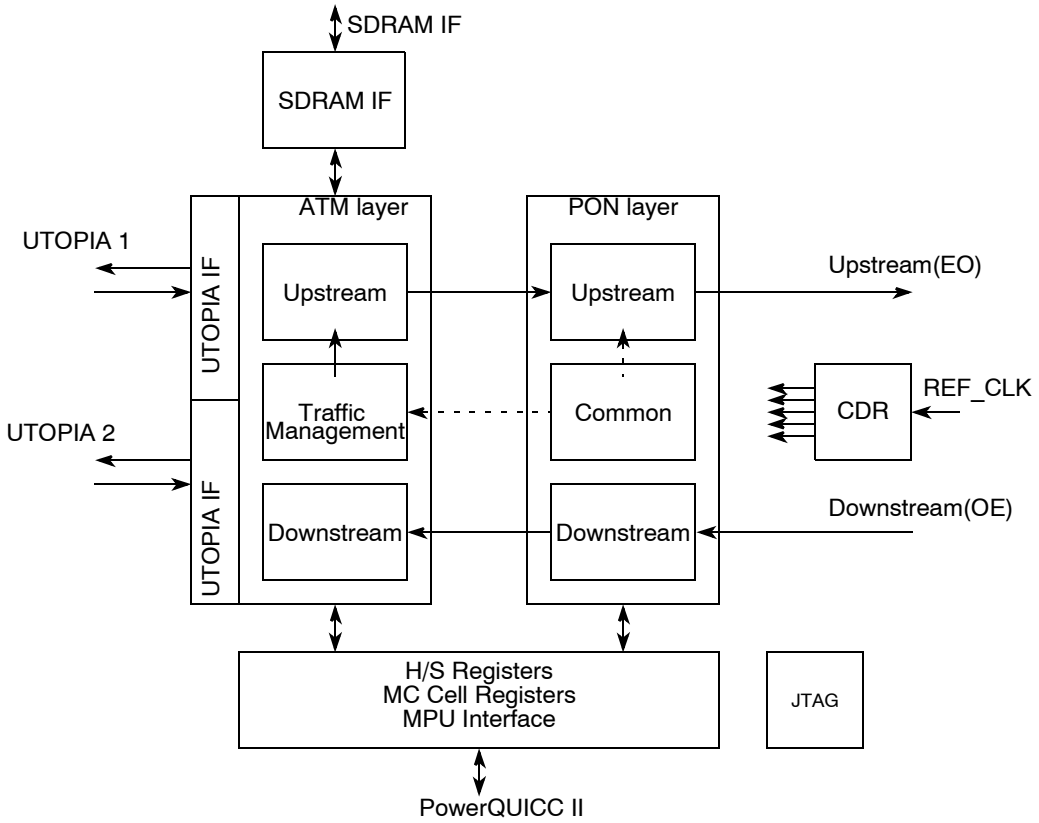


Figure 2. MC92701 BPON Layer Termination Device Block Diagram

2.3 Clock and Data Recovery (CDR)

The CDR module of the MC92701 BPON layer termination device extracts a clock signal from 155.52 Mbps or 622.08 Mbps downstream data. The recovered clock is divided to provide several internal clocks. An external reference clock source of 19.44 MHz ± 20 ppm is used.

2.3.1 Clock Signal Characteristics

All output and internal signals are generated based on PON_CLK, which is produced by the CDR. The characteristics of the clock signals are listed as follows:

- Jitter tolerance
  - ITU-T G.983.1 8.2.8.7.2 jitter tolerance
- Jitter transfer
  - ITU-T G.983.1 8.2.8.7.1 jitter transfer
- Jitter generation
  - ITU-T G.983.1 8.2.8.7.3 jitter generation

2.4 PON Layer

The following sections describe downstream and upstream processing of the PON layer. Common blocks for this layer are also described.

To send the signal to the OLT, the ATM block executes the multiplexing operation through the ATM layer function by collecting the ATM cells. The traffic management function and the processor follow the multiplexing by generating the divided_slot and the MC cell, respectively. A PON header is added before the signal is sent to OLT.

PON downstream and upstream processing have the following features in common:

- Multi-grant operation
- ONU state management
- BIP calculation

2.4.1 PON Downstream Processing

The PON downstream block delineates the ATM cell from the serial bit stream, which is sent from the OLT, to establish synchronization of the PLOAM and FRAME cells. In response to the OLT and the MPU, the extracted PLOAM in the PON downstream block is decoded and sent to the COMMON block. The PON downstream block includes function bit-interleave parity (BIP), ATM header correction, and filtering of user and MC cells. The user and MC cells are sent to the ATM layer and H/S interface block, respectively.

PON downstream processing is characterized by the following features:

- Cell delineation
- De-scramble
- Frame/PLOAM delineation
- Header correction
- De-churning
- VP/VC filter, cell MUX

2.4.2 PON Upstream Processing

The PON upstream block multiplexes the ATM cells that are collected by the ATM layer processing block, divided_slot, MC cells, and PLOAM cell. The divided_slot, MC cells, and PLOAM cell are generated by the traffic management block, the processor, and the message trigger from the common block or system. Once multiplexing is complete, a PON header is added before the ATM cells are sent out to the OLT. The PON upstream block also operates header error correction (HEC), bit interleaved parity (BIP), and scrambler for the ATM cell. Upstream scrambling and NRZ coding are performed in the PON layer. In addition, the PON layer controls the delay time of the ATM cell transmission.

PON upstream processing is characterized by the following features:

- Cell transmission delay
- Overhead insertion
- HEC calculation
- Scramble
- Churning key generation
- Upstream message generation

2.4.3 Performance of PON Downstream and Upstream Processing

Table 1 shows the performance of each feature of PON downstream and upstream processing.

Table 1. PON Downstream and Upstream Processing Performance

Feature	Description
Bit rate	Downstream: 622.08 Mbps/155.52 Mbps Upstream:155.52 Mbps
OLT-ONU distance	0–20 Km
Downstream frame sync	ITU-T G.983.1-compliant PLOAM CELL frame bit 155.52 Mbps: 56 cells x 53 bytes x 8 bits (153 μsec) 622.08 Mbps: 224 cells x 53 bytes x 8 bits (153 μsec)
Downstream scramble	ITU-T I.432.1-compliant Cell redundant sample scramble
Upstream traffic control	ITU-T G.983.2-compliant ITU-T G.983.4-compliant ITU-T G.983.7-compliant T-CONT type1 to 5 service
Upstream header	ITU-T G.983.1-compliant 3-byte PON-OH Guadband + Preamble + Delimitter
Upstream scramble	ITU-T G.983.1-compliant Reset type of each cell scramble Scramble $X^9 + X^4 + 1$
Minimum delay of ONU	7 to 9 cells @155.52 Mbps

2.4.4 Common Block

The common block decodes the PLOAM cell from the PON downstream block. It manages the ONU state machine, generates a trigger of indications, and sends the status to the upstream block, downstream block, and H/S register block.

2.5 ATM Layer Block

The ATM block has three major functions—virtual path identifier (VPI)/virtual channel identifier (VCI) connection conversion, OAM insert/drop, and traffic management. The PON layer function sends a filter consisting of the ATM cell header VPI value through the ATM layer. The ATM cell header is then sent out to a UTOPIA. Due to the differences in data transfer rates (155 Mbps and 622 Mbps), the downstream data is affected by back pressure. This pressure is relieved by using the external receive cells memory.

Upstream ATM cells received from the UTOPIA interface are classified according to T-CONT and accommodated in local memory.

The ATM layer performs OAM insert/drop. There are eight connections in each UTOPIA and two UTOPIA interfaces. Therefore, the OAM controls are applied to a total of 16 connections. In addition, the OAM function works independently from the PON layer. Table 2 shows the different kinds of OAM cells that are supported by the ATM layer block.

The ATM layer block also provides traffic management that is based on a dynamic bandwidth assignment (ITU-T G.983.4). The upstream cell is classified as QoS according to the ATM layer. The data is queued in external SDRAM local memory by the traffic management block. An internal data grant is processed by the PON layer along with priority control (WRR,SRR,HOL), and a cell is sent out from a suitable QoS buffer. The ATM layer block can set four QoS per UTOPIA and enable priority control by flexible logical connections of QoS, priority queue, and T-CONT.

Table 2. OAM Support

OAM	Flow	E-E/SEG	Downstream	Upstream	Comment
			Drop Point	Insert Point	
AIS	VP[F4]	E–E	8	—	Alarm indication signal E-E only
		SEG	—	—	
	VC[F5]	E–E	8	—	
		SEG	—	—	
RDI	VP[F4]	E–E	8	8	Remote defect indication E-E only
		SEG	—	—	
	VC[F5]	E–E	8	8	
		SEG	—	—	
CC	VP[F4]	E–E	8	8	Continuity check E-E/Seg independent
		SEG	8	8	
	VC[F5]	E–E	8	8	
		SEG	8	8	
LB	VP[F4]	E–E	1	1	Loopback (Ins/Drop)
		SEG	1	1	
	VC[F5]	E–E	1	1	
		SEG	1	1	
LBLB	VP[F4]	E–E	8	8	Loopback (Loopback point)
		SEG	8	8	
	VC[F5]	E–E	8	8	
		SEG	8	8	
ACT/DACT	VP[F4]	E–E	8	1	Activation/deactivation cell
		SEG	8	1	
	VC[F5]	E–E	8	1	
		SEG	8	1	
OPT	VP[F4]	E–E	1	1	Optional cell
		SEG	1	1	
	VC[F5]	E–E	1	1	
		SEG	1	1	

2.5.1 ATM Downstream Processing

The ATM downstream block filters the VPI/VCI values of the header, which are sent from the PON layer. To absorb the backpressure of 155-Mpbs bandwidth UTOPIAs during 622-Mbps downstream operation, the ATM layer temporarily stores downstream cells in the external SDRAM. The block gives higher priority to ATM cells of high priority QoS.

2.5.2 ATM Upstream Processing

In the ATM layer, traffic management logic performs QoS type classification on the upstream cells and stores them in the external SDRAM. It also performs a priority management (WRR, SRR, HOL) by its own data grant that is processed at PON layer. Then these cells are transmitted from the appropriate QoS buffer.

In each UTOPIA a maximum of four QoS can be configured. Priority management is achieved by a logical connection of QoS/priority and queue/TCONT.

2.6 Other Interfaces

The following sections describe other interfaces for the MC92701 BPON layer termination device.

2.6.1 SDRAM Interface

The SDRAM interface accesses external SDRAM under the control of the ATM layer and PON layer blocks.

2.6.2 UTOPIA Interface

ATM cells pass between an external PowerQUICC communications processor and the MC92701 through the Utopia Interface. Two UTOPIA level 1-compliant interfaces are available to support two channels of 155 Mbps.

The UTOPIA interface block transmits ATM cells which are received from the ATM downstream block. OAM drop processing is performed by matching the connection number (CN) for received ATM cells in this block. It supports the OAM functions —AIS,RDI, CC, E-E, LB, LBLB, ACT, DACT, and OPT. Additionally, user cells are switched by VPI/VCI.

The UTOPIA block decodes and manages the CN number and QoS number from the VPI/VCI value in the ATM cells to determine which ATM cells are sent next to the upstream block. Also, OAM insertion processing is performed in the block for each CN number. OAM insertion processing supports the OAM functions—AIS,RDI, CC, E-E, LB, LBLB, ACT, DACT, and OPT.

2.6.3 Hardware/Software (H/S) Registers

ONT status and ONT management information is contained in H/S registers which are accessed through the MPU interface to manage and debug the ONT.

2.6.4 Management and Control (MC) Cell Registers

The MC cell registers store ITU-T G983.2 format compliant, one-cell concluded type OMCC format MC cells for interface to the external PowerQUICC communications processor.

Downstream ATM cells which match the VP/VC value assigned by a downstream PLOAM message as OMCC cells are extracted from the ATM cell flow. Upstream OMCC cells are inserted from MC cell registers at the rate requested by the MAC layer in the OLT under control of the traffic management block.

2.6.5 MPU Interface

The MC92701 MPU interface is a slave interface providing access to internal H/S registers and memory from an external PowerQUICC communications processor.

2.6.6 Design for Test Functions

MC92701 BPON layer termination device has the following built-in test functions:

. • Boundary scan test (IEEE1194-1 JTAG)—supports on-board continuity test.

. • PLL BIST—runs self test on Analog PLL in order to check its functionality and performance.

. • RAM BIST—runs self test on internal memories to check its functionality and performance.

. • Internal scan test

3 MC92701 BPON Layer Termination Device Applications

The MC92701 BPON layer termination device can be used for the following applications:

- FTTH/FTTC/FTTB

4 Document Revision History

Table 3 provides a revision history for this product brief.

Table 3. Document Revision History

Revision Number	Substantive Change(s)
0	Initial release.
1	Overview section modified

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

HOW TO REACH US

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE:

http://motorola.com/semiconductors

MOTOROLA

MC92701PB/D