UNIVERSAL
4-BIT SHIFT REGISTER

MC9300L*
MC8300L,P*

Input Loading Factor
J, $\overline{K}$, $\overline{MR}$, D_{P0}, D_{P1}, D_{P2}, D_{P3} = 1
$\overline{PE}$ = 2.3
Clock = 4

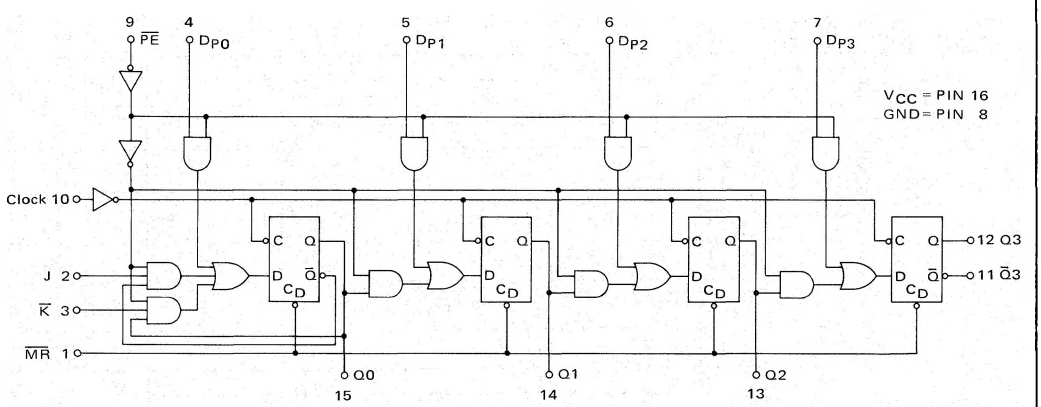
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg

Propagation Delay Time = 25 ns typ

This serial/parallel shift register consists of four flip-flops operated in the synchronous mode. Functions available are shift left, shift right, serial-to-serial, parallel-to-parallel, serial to-parallel, and parallel-to-serial conversion.

This device operates on the positive-going edge of the clock pulse in both the serial and parallel mode. The device includes an internal clock buffer, input clamp diodes to reduce ringing, Q outputs for all four stages, $\overline{Q}$ output for the last stage, synchronous parallel entry, and an asychronous master reset. The J and $\overline{K}$ inputs are available, and may be tied together to produce a D input.



INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9300 INPUT LOADING FACTOR	MC9300 OUTPUT LOADING FACTOR
MC9300	1.0	6
MC500	1.06	6.4
MC2100	0.7	4.25
MC3100	0.7	3.6
MC4300	1.0	4.65
MC5400	1.0	4.65
MC930**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	5.6

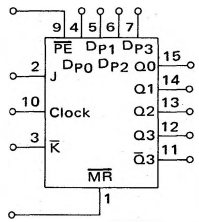
FAMILY	MC8300 INPUT LOADING FACTOR	MC8300 OUTPUT LOADING FACTOR
MC8300	1.0	6
MC400	1.0	5.45
MC2000	0.6	4.5
MC3000	0.7	4.25
MC4000	1.0	5.3
MC7400	1.0	5.3
MC830**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	6.1

**Due to logic "1" state drive limitations of the MDTL family.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one parallel data input. Other parallel data inputs are tested in the same manner. Further, test procedures are shown for only one output. Complete testing according to the Functional Test Diagram.

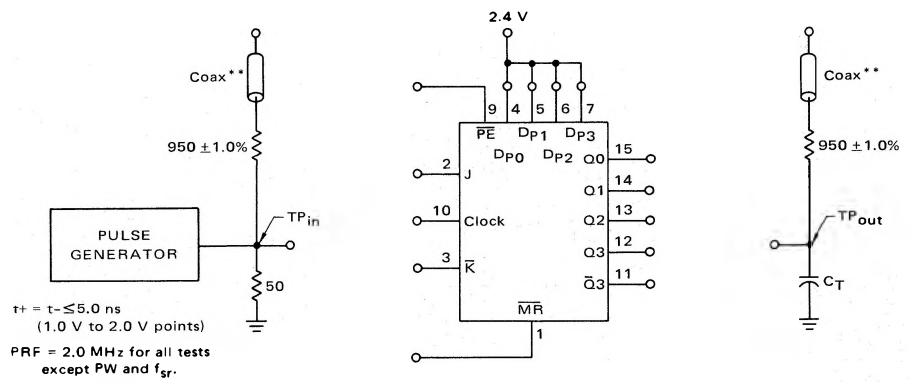


@ Test Temperature		TEST CURRENT/VOLTAGE VALUE mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9300	−55°C	9.6	7.44	−0.36	–	0.80	2.0	0.4	4.5	–	4.5	5.5
	+25°C	9.6	7.44	−0.36	−10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
	+125°C	9.6	7.44	−0.36	–	0.80	1.4	0.4	4.5	–	4.5	5.5
MC8300	0°C	9.6	8.5	−0.36	–	0.85	1.9	0.45	4.5	–	4.75	5.25
	+25°C	9.6	8.5	−0.36	−10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
	+75°C	9.6	8.5	−0.36	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9300 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8300 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																												
Forward Current — $\overline{MR}$	I_{F1}	1	–	−1.6	–	−1.6	–	−1.6	mAdc	–	−1.6	–	−1.6	–	−1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	1	–	2	–	–	–	↓	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	4	3	–	–	–	↓	1	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	4	–	–	–	↓	–	↓
$\overline{PE}$		9	–	−3.68	–	−3.68	–	−3.68	↓	–	−3.68	–	−3.68	–	−3.68	↓	–	–	–	–	–	–	9	–	–	–	↓	–	↓
Clock		10	–	−6.4	–	−6.4	–	−6.4	↓	–	−6.4	–	−6.4	–	−6.4	↓	–	–	–	–	–	–	10	–	–	–	↓	–	↓
$\overline{MR}$	I_{F2}	1	–	−1.24	–	−1.24	–	−1.24	mAdc	–	−1.41	–	−1.41	–	−1.41	mAdc	–	–	–	–	–	–	1	–	–	16	–	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	1	–	2	–	–	–	–	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	4	3	–	–	–	–	1	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	4	–	–	–	–	–	↓
$\overline{PE}$		9	–	−2.85	–	−2.85	–	−2.85	↓	–	−3.24	–	−3.24	–	−3.24	↓	–	–	–	–	–	–	9	–	–	–	–	–	↓
Clock		10	–	−4.95	–	−4.95	–	−4.95	↓	–	−5.65	–	−5.65	–	−5.65	↓	–	–	–	–	–	–	10	–	–	–	↓	–	↓
Leakage Current — $\overline{MR}$	I_R	1	–	60	–	60	–	60	μAdc	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	1	–	–	16	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	–	2	–	–	–	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	–	3	–	–	–	–	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	–	4	–	–	–	–	↓
$\overline{PE}$		9	–	140	–	140	–	140	↓	–	140	–	140	–	140	↓	–	–	–	–	–	–	–	9	–	–	–	–	↓
Clock		10	–	240	–	240	–	240	↓	–	240	–	240	–	240	↓	–	–	–	–	–	–	–	10	–	–	↓	–	↓
Clamp Voltage — $\overline{MR}$	V_D	1	–	–	–	−1.5	–	–	Vdc	–	–	–	−1.5	–	–	Vdc	–	–	–	1	–	–	–	–	–	16	–	–	8
J		2	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	2	–	–	–	–	–	↓	–	–	↓
$\overline{K}$		3	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	3	–	–	–	–	–	↓	–	–	↓
D_{P0}		4	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	4	–	–	–	–	–	↓	–	–	↓
$\overline{PE}$		9	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	9	–	–	–	–	–	↓	–	–	↓
Clock		10	–	–	–	–	–	–	↓	–	–	–	–	–	–	↓	–	–	–	10	–	–	–	–	–	–	–	–	↓
Output																												
Output Voltage	V_{OL}	12	–	0.4	–	0.4	–	0.4	Vdc	–	0.45	–	0.45	–	0.45	Vdc	12	–	–	–	4,5,6,7,9	–	–	–	–	–	16	1	8
		12	–	0.4	–	0.4	–	0.4	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	12	–	–	4,5,6,7,9	–	–	–	–	16	–	1	8
	V_{OH}	11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	–	4,5,6,7,9	–	–	–	–	16	–	1	8
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	16	–	–	–	75	–	–	mAdc	–	–	–	80	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	1,8

Pulse 1: V_{IH}, V_{IL}, 100 ns min

SWITCHING TIME TEST CIRCUIT



t+ = t-≤5.0 ns
(1.0 V to 2.0 V points)

PRF = 2.0 MHz for all tests except PW and f_{sr}.

Three pulse generators are required and must be slaved together to provide the waveforms shown.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

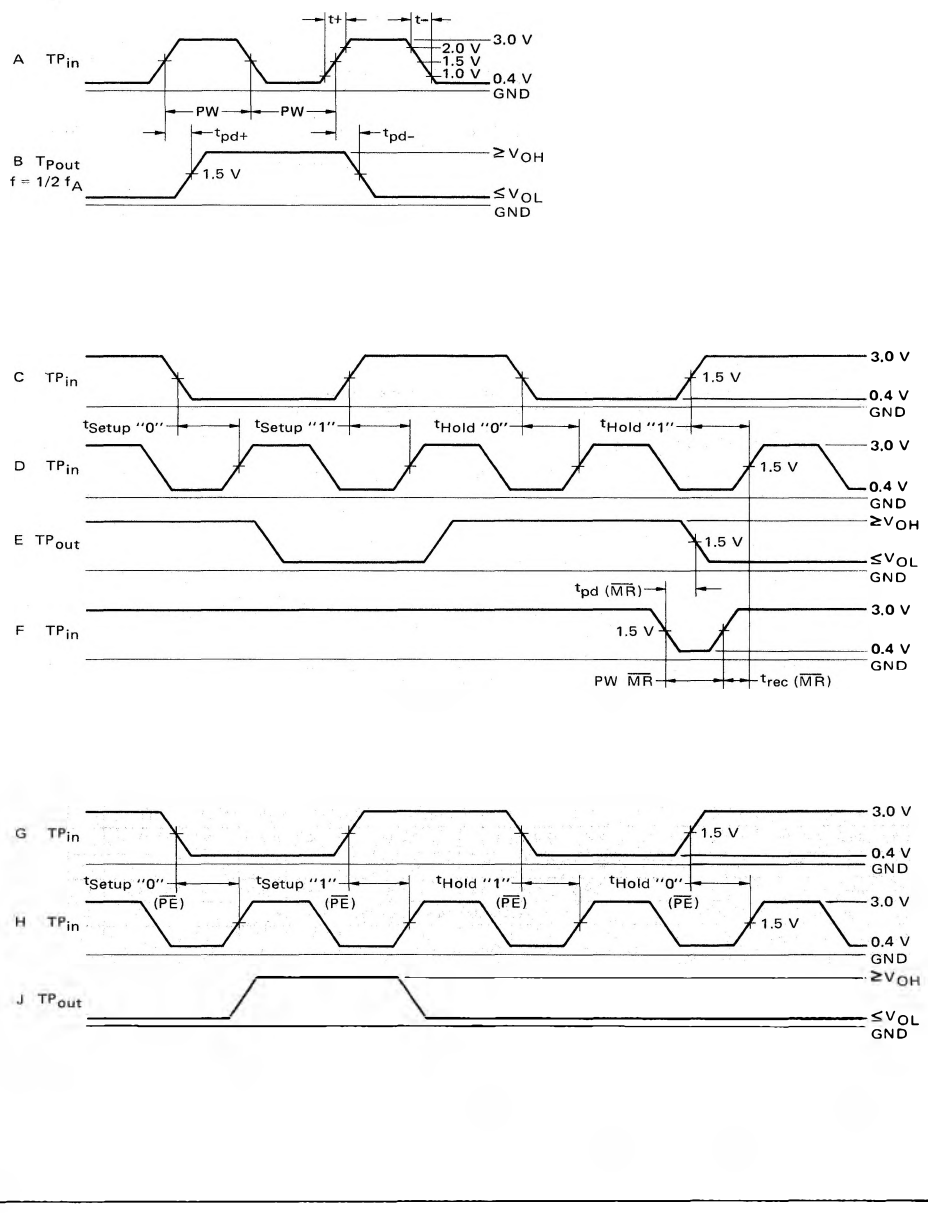
SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST	INPUT Pin 1 $\overline{MR}$	Pin 2 J	Pin 3 K	Pins 4, 5, 6 D_{P0}, D_{P1}, D_{P2}	Pin 7 D_{P3}	Pin 9 $\overline{PE}$	Pin 10 Clock	OUTPUT Pin 12 Q3	VALUE Min	Typ	Max	Unit
Turn-Off Delay, Clock to Q3	t_{pd+}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	–	18	35	ns
Turn-On Delay, Clock to Q3	t_{pd-}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	–	25	45	ns
Maximum Shift Rate	f_{sr}	12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	15	25	–	MHz
Minimum Clock Pulse Width	PW	Tested during each of the above tests.									–	13	35	ns
Minimum Data Input Setup Time (Serial or Parallel Inputs)	t_{Setup} "1" t_{Setup} "0"	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ①	–	14	35	ns
Maximum Data Input Hold Time (Serial or Parallel Inputs)	t_{Hold} "1" t_{Hold} "0"	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ②	0	16	–	ns
Minimum Recovery Time, $\overline{MR}$ Input	t_{rec}	Tested during Data Input t_{Setup} and t_{Hold} tests.									–	19	30	ns
Minimum $\overline{MR}$ Pulse Width	PW										–	15	30	ns
Turn-On Delay, $\overline{MR}$ to Q3	t_{pd-}	1,12	F	2.4 V	Gnd	2.4 V	2.4 V	Gnd	D	E	–	29	45	ns
Minimum $\overline{PE}$ Input Setup Time	t_{Setup} "1" t_{Setup} "0"	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ①	–	22	45	ns
Maximum $\overline{PE}$ Input Hold Time	t_{Hold} "1" t_{Hold} "0"	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ②	10	18	–	ns

① Output toggles. ② Output does not toggle.

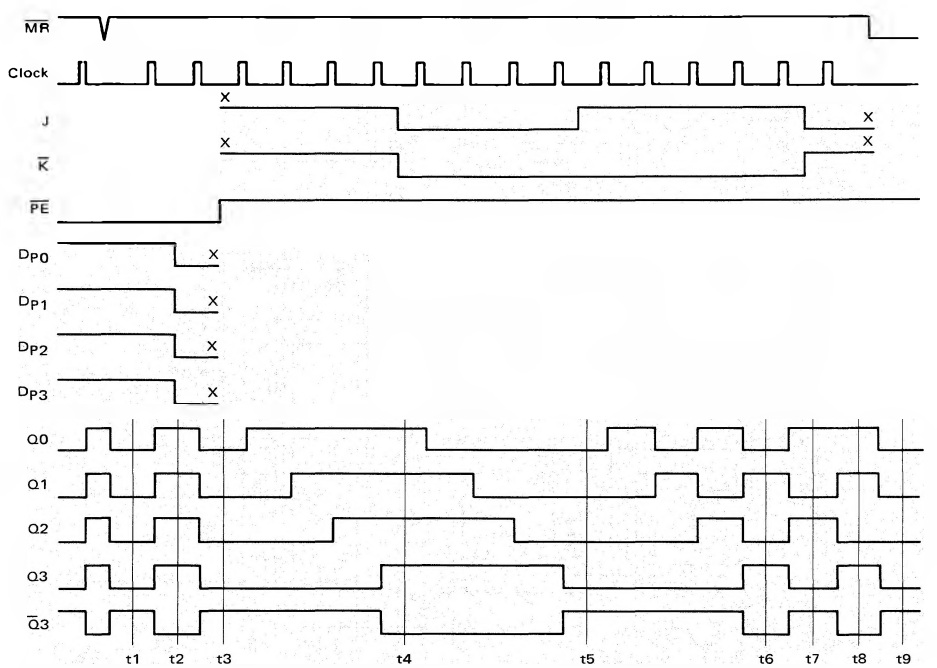
VOLTAGE WAVEFORMS



FUNCTIONAL DESCRIPTION

1. J and $\overline{K}$ inputs are made available on the first flip-flop of the register to provide full input logic capability without restrictions other than setup and release times. The simpler D type input can be obtained by wiring the J and $\overline{K}$ inputs together.
2. Parallel data inputs are provided to each stage of the register. These inputs are enabled only when the Parallel Enable is low. Information is transferred to the register on the positive transition of the clock. This information is shifted to the right on the next positive transition of the clock if the Parallel Enable is high. Shift left operation is achieved by driving the parallel inputs with the Q outputs of the right-adjacent stage. For this operation the Parallel Enable must be low.
3. An internal clock buffer has been included to reduce clock input loading, allowing the clock input of the register to be driven by a single gate.
4. The true output is provided for all stages; the complementary output is also provided for the last stage.
5. The master asynchronous $\overline{reset}$ input will clear the register independent of the conditions of the other inputs.

FUNCTIONAL DIAGRAM



X = Voltage level of unspecified area(s) preceding or following "X" are unimportant.

CIRCUIT SCHEMATIC