

PRESETTABLE
DECADE COUNTER

MC9300/MC8300 series

MC9310L*
MC8310L,P*

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

The MC9310/8310 decade counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

Input Loading Factors:

$\overline{MR}$, C_{EP} = 1

Clock, $\overline{PE}$, C_{ET} = 2

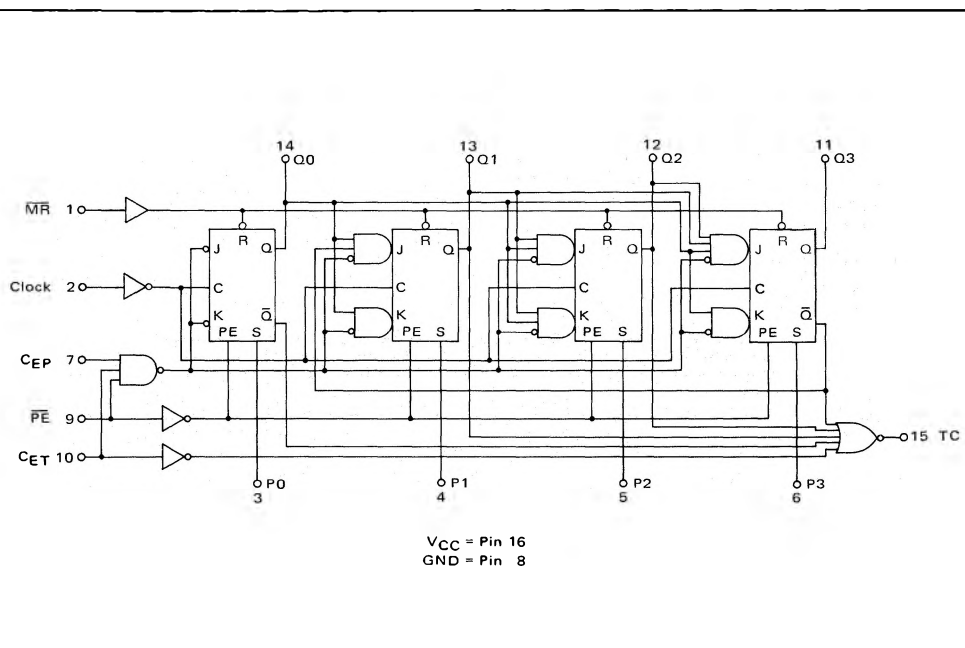
P0, P1, P2, P3 = 2/3

Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg

Propagation Delay Time = 14 to 35 ns typ

Toggle Frequency = 28 MHz typ



* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table.

1	MR	Q0	14
2	C		
3	P0	O1	13
4	P1		
5	P2	O2	12
6	P3		
7	CEP	O3	11
9	PE		
10	CET	TC	15

MC9310, MC8310 (continued)

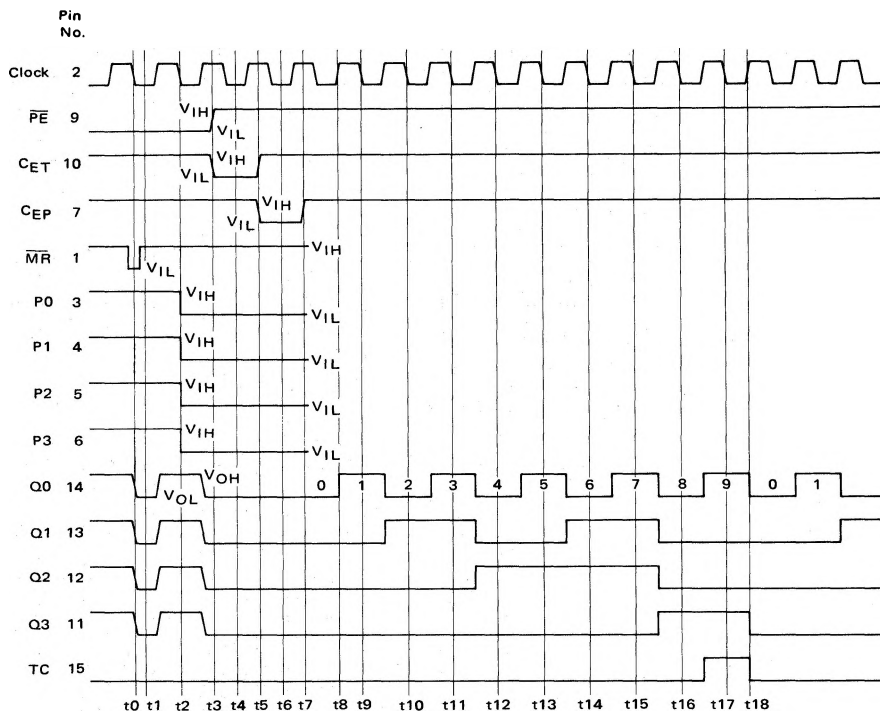
Characteristic		Pin Under Test		TEST CURRENT/VOLTAGE VALUES											
				mA						Volts					
				IOL1	IOL2	IOH	ID	VIL	VIH	VF	VR	VCC	VCCL	VCCCH	VCCCH
				@ Test Temperature											
Input Forward Current	IF	1 2 3		MC9310											
				-55°C											
				9.6	7.44	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	5.5
Leakage Current	IR	1 2 3		MC9310											
				-55°C											
				9.6	7.44	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	5.5
Clamp Voltage	VD	1		MC8310											
				-55°C											
				9.6	8.50	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25	5.25
Output Voltage	VOL1 VOL2 VOH	11 11 11		MC8310											
				-55°C											
				11	11	11	11	11	11	11	11	11	11	11	11
Power Requirements (Total Device) Power Supply Drain Current	IPD	16		MC8310											
				-55°C											
				11	11	11	11	11	11	11	11	11	11	11	11
Switching Parameters Turn-On Delay - Q	tPD+	2,14		MC8310											
				-55°C											
				2	2	2	2	2	2	2	2	2	2	2	2
Turn-Off Delay - Q	tPD-	2,15		MC8310											
				-55°C											
				2	2	2	2	2	2	2	2	2	2	2	2
Turn-On Delay - TC	tPD+	2,15		MC8310											
				-55°C											
				2	2	2	2	2	2	2	2	2	2	2	2

* Apply after potentials have been applied to other pins.

VR (Hold) Gnd ≥50 ns

MC9310, MC8310 (continued)

TIMING DIAGRAM

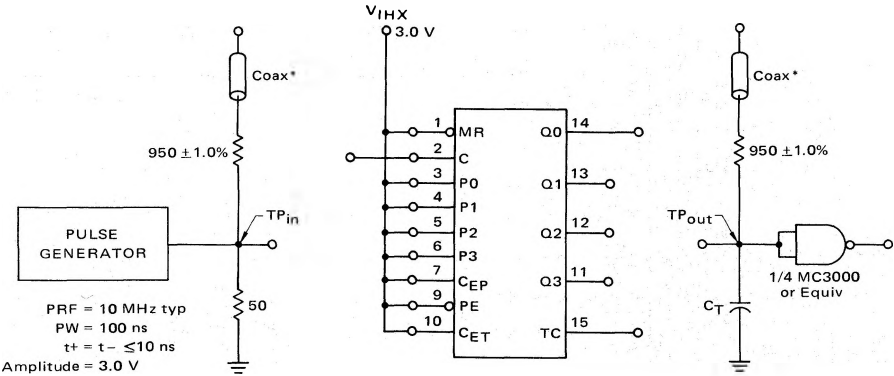


NOTES

- The Clock pulse must be in the high state during the high to low transition of CET and CEP , and the low to high transition of PE for correct logic operation.
- Pin conditions reflected on timing diagram for tests at time specified:
 - t_0 : Parallel (P) inputs high, Parallel Enable (PE) low, asynchronous Master Reset (MR) pulsed; Q outputs make transition from high to low.
 - t_1 : Measure both V_{OL1} and V_{OL2} on Q0, Q1, Q2, Q3 and TC before Clock goes high.
 - t_2 : Clock has been pulsed, Q outputs are high; measure V_{OH} .
 - t_3 : Clock is in high state while transitions of PE and CET occur (necessary condition). Parallel entry is now inhibited, P inputs are at the low level.
 - t_4 : Count enable (CET) is at the low level (disabled), count cannot occur; check Q outputs to see that they remain at the low level.
 - t_5 : CET is set to a high level and CEP is set at the low level while the Clock is high.
 - t_6 : Check Q outputs to see that count is disabled, outputs remain low.
 - t_7 : CEP is set high while Clock is high; count is now enabled.
 - t_8 : Clock is pulsed, count begins from 0000 to 0001.
 - t_9 thru t_{17} : Check Q and TC output states.
 - t_{18} : Outputs go to low state, count begins (0000).

MC9310, MC8310 (continued)

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

