

PRESETTABLE
4-BIT BINARY COUNTER

MC9300/MC8300 series

MC9316L*
MC8316L,P*

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Input Loading Factors:

MR, C_{EP} = 1

Clock, P_E, C_{ET} = 2

P₀, P₁, P₂, P₃ = 2/3

Output Loading Factor = 6

The MC9316/8316 hexadecimal counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

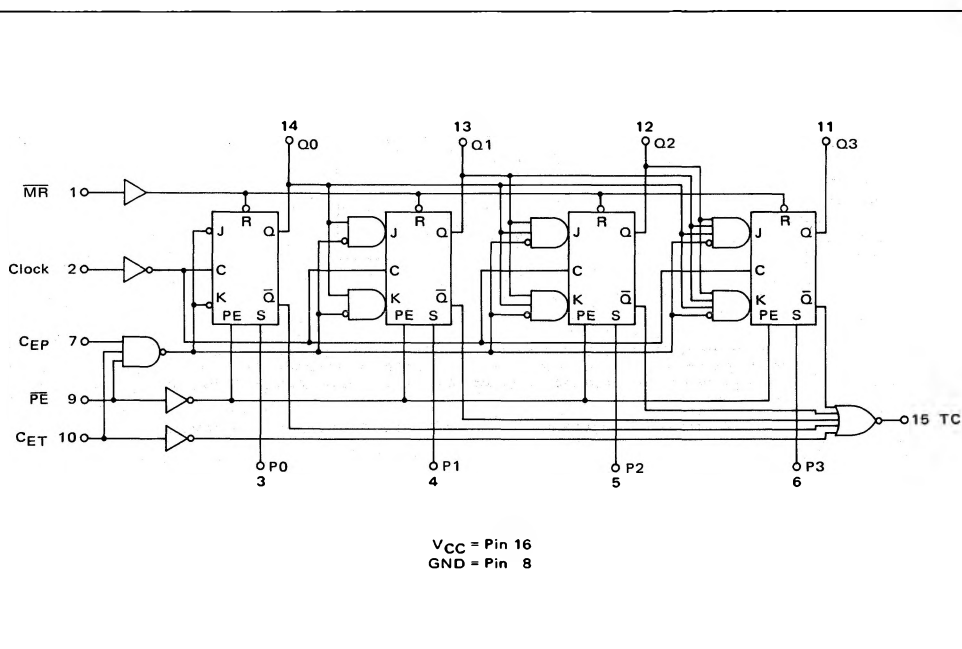
An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

Total Power Dissipation = 300 mW typ/pkg

Propagation Delay Time = 14 to 35 ns typ

Toggle Frequency = 28 MHz typ



*L suffix = 16-pin dual in-line ceramic package (Case 620).

P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table.

MC9316, MC8316 (continued)

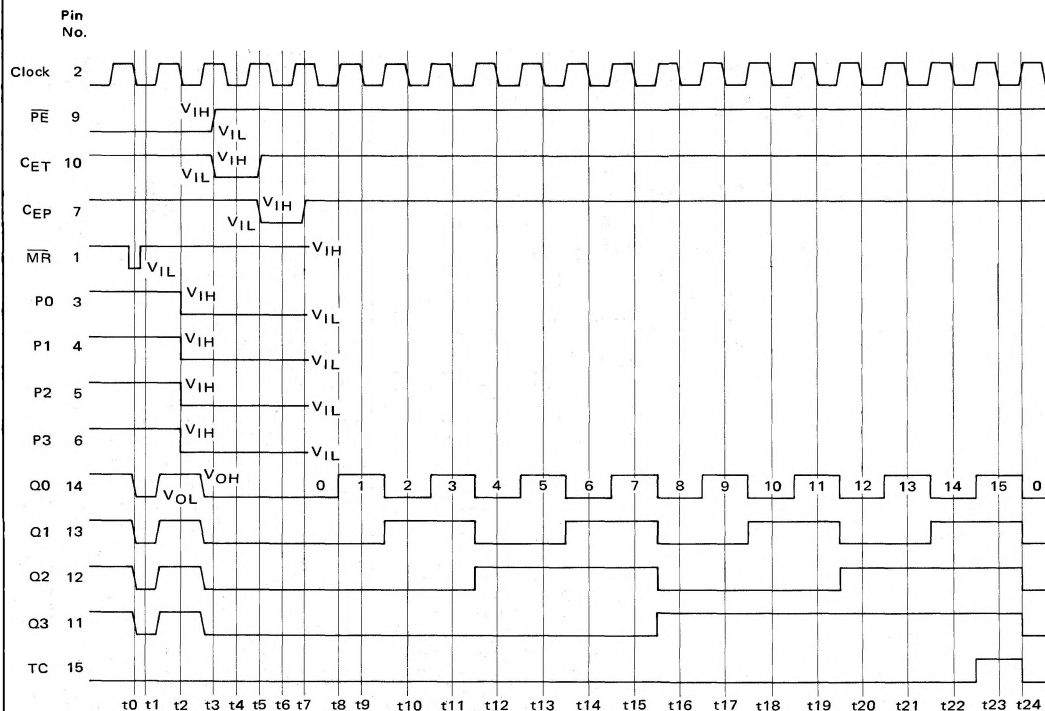
1	MR	Q0	14	-
2	Clock			
3	P0	Q1	13	
4	P1			
5	P2	Q2	12	
6	P3			
7	C _{EP}	Q3	11	
9	PE			
10	C _{ET}	TC	15	

TEST CURRENT/VOLTAGE VALUES			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
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			I _{OL1}	I _{OL2}	I _{OH}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{CC}	V _{CLL}	V _{CC}	V _{CH}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
Input	Forward Current	I _F	1	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-

* Apply after potentials have been applied to other pins. V_R (Hold) $\overline{\text{Gnd}} \geq 50 \text{ ns}$

MC9316, MC8316 (continued)

TIMING DIAGRAM

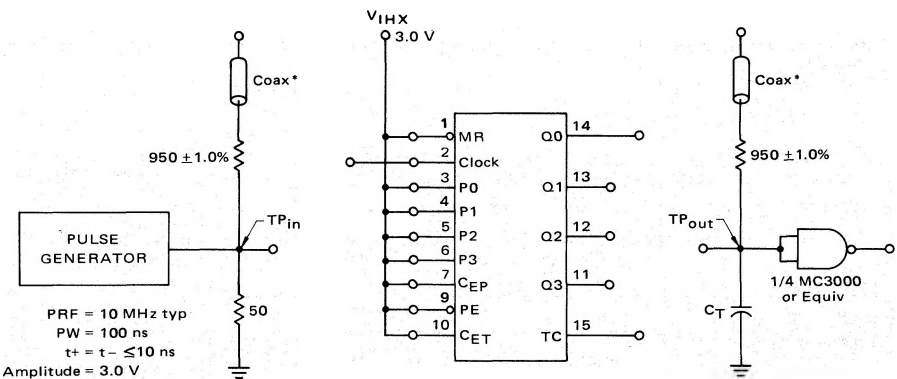


NOTES

- The Clock pulse must be in the high state during the high to low transition of CET and CEP , and the low to high transition of $\overline{PE}$ for correct logic operation.
- Pin conditions reflected on timing diagram for tests at time specified:
 - t_0 : Parallel (P) inputs high, $\overline{PE}$ low, asynchronous Master Reset ($\overline{MR}$) pulsed; Q outputs make transition from high to low.
 - t_1 : Measure both V_{OL1} and V_{OL2} on $Q0, Q1, Q2, Q3$ and TC before Clock goes high.
 - t_2 : Clock has been pulsed, Q outputs are high; measure V_{OH} .
 - t_3 : Clock is in high state while transitions of $\overline{PE}$ and CET occur (necessary condition). Parallel entry is now inhibited, P inputs are at the low level.

- Count enable (CET) is at the low level (disabled), count cannot occur; check Q outputs to see that they remain at the low level.
- CET is set to a high level and CEP is set at the low level while the Clock is high.
- Check Q outputs to see that count is disabled, outputs remain low.
- CEP is set high while Clock is high; count is now enabled.
- Clock is pulsed, count begins from 0000 to 0001.
- Check Q and TC output states.
- Outputs go to low state, count begins (0000).

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



$C_T = 15$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

