OPERATIONAL AMPLIFIERS

MCBC1741 MCB1741F

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1741 and MCB1741F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

MAXIMUM RATINGS (T_A = $+25^{\circ}$ C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	v⁺	+22	Vdc
	V-	-22	
Differential Input Signal	Vin	±30	Volts
Common Mode Input Swing (Note 1)	CMVin	±15	Volts
Output Short Circuit Duration (Note 2)	ts ,	Continuous	
Power Dissipation	PD	500	mW
Derate above $T_A = +25^{\circ}C$ (Flat Package)		3.3	mW/ ⁰ C
Operating Temperature Range	TA	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Note 1. For supply voltages less than \pm 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.





This is advance information on a new introduction and specifications are subject to change without notice. See Packaging Information Section for outline dimensions.





MCBC1741, MCB1741F (continued)

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25^oC unless otherwise noted)

Characteristic		MCBC1741, MCB1741F			_
	Symbol	Min	Тур	Max	Unit
Open Loop Voltage Gain (R _L = 2.0 kΩ) (V _O = ±10 V, T _A = +25 ^O C) (V _O = ± 10 V, T _A = -55 to +125 ^O C)	AVOL	50,000 25,000	200,000		-
Output Impedance (f = 20 Hz)	Zo		75		Ω
Input Impedance (f = 20 Hz)	Z _{in}	0.3	1.0	_	MegΩ
Output Voltage Swing (R _L = 10 k Ω) (R _L = 2.0 k Ω) (R _L = 2.0 k Ω , T _A = -55 to +125 ^o C)	Vo	±12 ±10 ±10	±14 ±13 -		Vpeak
Input Common-Mode Voltage Swing	CMV _{in}	±12	±13	_	V _{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM _{rej}	70	90	_	dB
Input Bias Current ($T_A = +25^{\circ}C$) ($T_A = -55^{\circ}C$)	۱ _۵	-	0.2 0.5	0.5 1.5	μΑ
Input Offset Current ($T_A = +25^{\circ}C$) ($T_A = -55$ to +125°C)	lliol	-	0.03	0.2 0.5	μA
Input Offset Voltage $(T_A = +25^{\circ}C)$ $(T_A = -55^{\circ}C \text{ to } +125^{\circ}C)$	V _{io}	- -	1.0	5.0 6.0	mV
Step Response Gain = 100, R ₁ = 1.0 kΩ, R ₂ = 100 kΩ, R ₃ = 1.0 kΩ	tf tpd dV _{out} /dt ①	- -	29 8.5 1.0	- - -	μs μs V/μs
Gain = 10, R ₁ = 1.0 kΩ, R ₂ = 10 kΩ, R ₃ = 1.0 kΩ	t _f tpd dV _{out} /dt ①	- - -	3.0 1.0 1.0	- - -	μs μs V/μs
Gain = 1, R ₁ = 10 kΩ, R ₂ = 10 kΩ, R ₃ = 5.0 kΩ	t _f t _{pd} dV _{out} /dt ①		0.6 0.38 0.8		μs μs V/μs
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50 \Omega, TA = -55^{\circ}C$ to +125 ^o C) ($R_S = 10 k\Omega, T_A = -55^{\circ}C$ to +125 ^o C)	TC _{Vio}		3.0 6.0	-	µ∨/ºC
Average Temperature Coefficient of Input Offset Current (T _A = -55 to +125 ⁰ C)	tc _{Vio}	-	50	_	pA/ ^o C
DC Power Dissipation (Power Supply = ±15 V, V ₀ = 0)	۴ _D	-	50	85	mW
Positive Supply Sensitivity (V ⁻ constant)	\$ ⁺		30	150	μV/V
Negative Supply Sensitivity (V ⁺ constant)	s⁻	_	30	150	μ <u>ν</u> /ν
Power Bandwidth (Α _v = 1, R _L = 2.0 kΩ, THD = 5%, V _o = 20 V _{P·P})	PBW	_	10	-	kHz

1 dVout/dt = Slew Rate



$$\label{eq:transformation} \begin{split} \textbf{TYPICAL CHARACTERISTICS (continued)} \\ (V^{+} = +15 \ Vdc, \ V^{-} = -15 \ Vdc, \ T_{A} = +25^{O}C \ unless \ otherwise \ noted.) \end{split}$$



TYPICAL CHARACTERISTICS (continued) ($V^* = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted.)

FIGURE 11 - BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal

PACKAGING AND HANDLING

The MCBC1741 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.