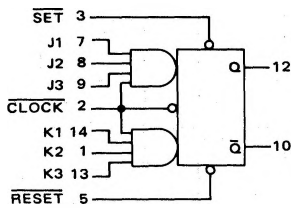
J-K FLIP-FLOP

MCBC5472*
MCB5472F*

BEAM LEAD

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. $\overline{SET}$ and $\overline{RESET}$ inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs. Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

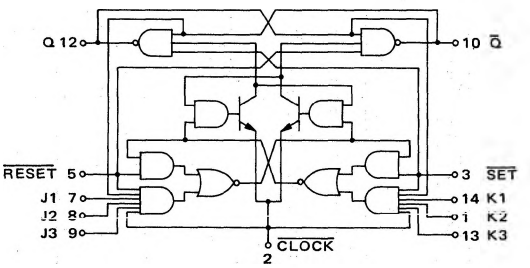
$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

Input Loading Factor:
J, K = 1
$\overline{CLOCK}$, $\overline{SET}$, $\overline{RESET}$ = 2

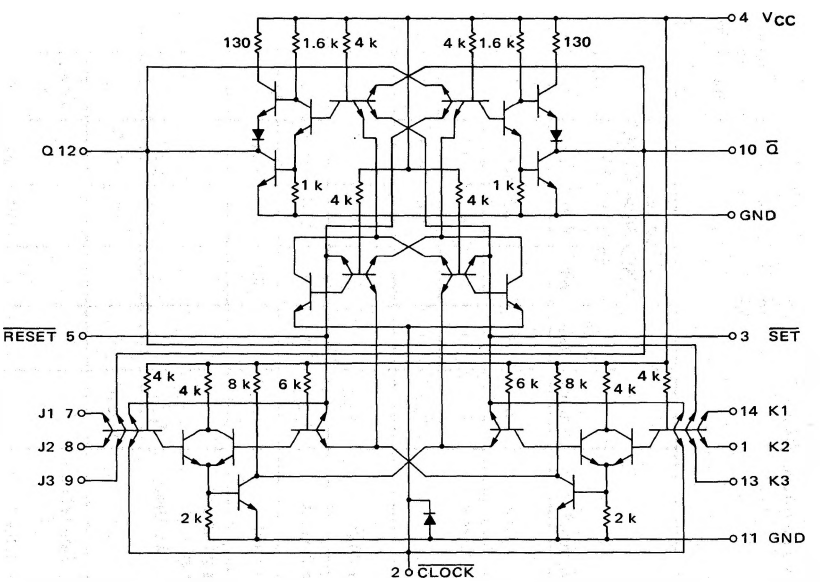
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 30 ns typ
Max Operating Frequency = 20 MHz typ

LOGIC DIAGRAM



Package No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Beam No.	1	2	3	4	5	6	7	9	10	11	12	13	14	15



*F suffix = 1/4" x 1/4" ceramic package (Case 651) MCBC-prefixed devices are unencapsulated. See General Information section for package and chip details.

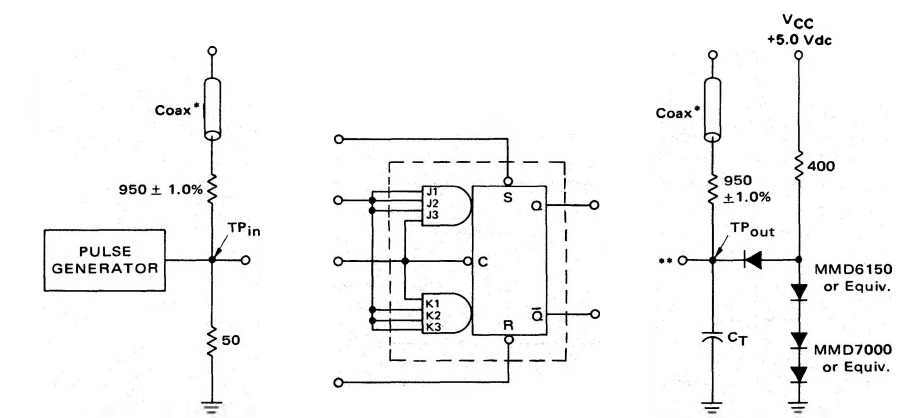
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state, and application of a logic "0" to the $\overline{RESET}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{SET}$ and $\overline{RESET}$ inputs override the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t− = 6 ns } 10% to 90% points
f = 10 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and $\overline{CLOCK}$ tests.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

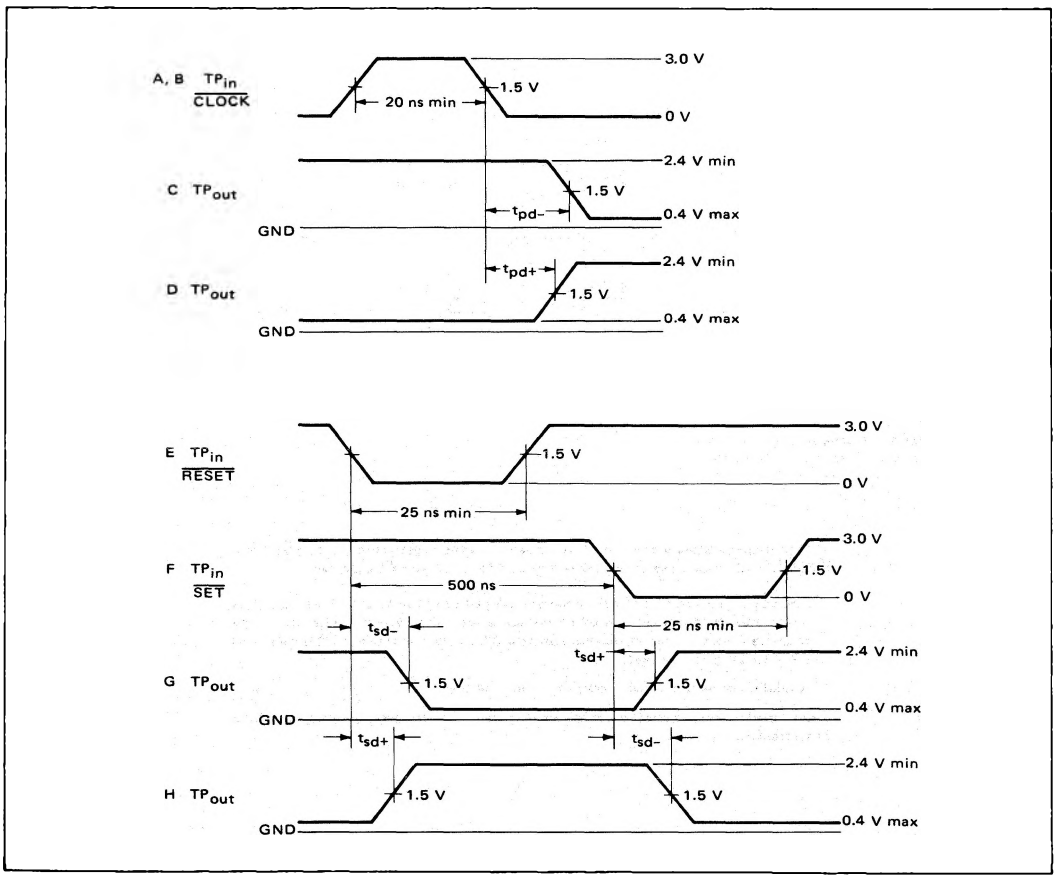
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	C	10	40	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	D	D	10	25	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	–	40	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	–	25	ns
Enable Voltage	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

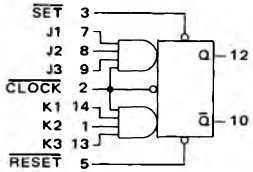
†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and $\overline{CLOCK}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



Characteristic		Symbol	Pin Under Test	Test Limits MCBC5472/MCBC5472F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_R (Volts)	V_{th1} (Volts)	V_{th0} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
							TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
							16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5	
Input																	
Forward Current	J	I_F	7	-	-1.6	mAdc	-	-	7	-	-	2,5*,8,9	-	-	-	4	11
	K		14	-	-1.6		-	-	14	-	-	1,2,3*,13	-	-	-		
	$\overline{Set}$		3	-	-3.2		-	-	3	-	-	1,2,7,8,9,13,14	-	-	-		
	$\overline{Reset}$		5	-	↓	↓	-	-	5	-	-	1,2,7,8,9,13,14	-	-	-		
	$\overline{Clock}$		2	-			-	-	2	-	-	1,5*,7,8,9,13,14	-	-	-		
			2	-			-	-	2	-	-	1,3*,7,8,9,13,14	-	-	-	↓	
Leakage Current	J	I_{R1}	7	-	40	μAdc	-	-	-	7	-	-	-	-	-	4	2,5,8,9,11
	K		14	-	40		-	-	-	14	-	-	-	-	-		1,2,3,11,13
	$\overline{Set}$		3	-	80		-	-	-	3	-	-	-	-	-		2,7,8,9,11
	$\overline{Reset}$		5	-	↓	↓	-	-	-	5	-	-	-	-	-		1,2,11,13,14
	$\overline{Clock}$		2**	-			-	-	-	2	-	-	-	-	-	↓	1,2,5,7,8,9,11,13,14
	J	I_{R2}	7	-	1.0	mAdc	-	-	-	-	7	-	-	-	-	4	2,5,8,9,11
	K		14	-	↓	↓	-	-	-	-	14	-	-	-	-		1,2,3,11,13
	$\overline{Set}$		3	-			-	-	-	-	3	-	-	-	-		2,7,8,9,11
	$\overline{Reset}$		5	-			-	-	-	-	5	-	-	-	-		1,2,11,13,14
	$\overline{Clock}$		2	-			-	-	-	-	2	-	-	-	-	↓	1,3,5,7,8,9,11,13,14
Output																	
Output Voltage		V_{OL}	10	-	0.4	Vdc	10	-	-	-	-	-	5	3	4	-	11
			12	-	0.4	Vdc	12	-	-	-	-	-	3	5	4	-	11
		V_{OH}	10	2.4	-	Vdc	-	10	-	-	-	-	3	5	4	-	11
			12	2.4	-	Vdc	-	12	-	-	-	-	5	3	4	-	11
Short-Circuit Current		I_{SC}	10	-20	-57	mAdc	-	-	-	-	-	1,7,8,9,13,14	-	-	-	4	2,5,10,11
			12	-20	-57	mAdc	-	-	-	-	-	1,7,8,9,13,14	-	-	-	4	2,3,11,12
Power Requirements																	
Power Supply Drain		I_{PD}	4	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	5,11
			4	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	3,11

*Momentarily ground pin prior to taking measurement.
**Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.