

MCB5401F*

MCBC5400/MCB5400F series

BEAM LEAD



This device consists of four 2-input NAND gates with no output pullup network that is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques, or standard flat package assembly techniques.



VOLTAGE WAVEFORMS AND DEFINITIONS

SWITCHING TIME TEST CIRCUIT



*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

STICS
ISTI
ERIS'
ARA
L CHARACT
AL
TRICAL
LECT
Ξ

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through re-maining inputs.

e,	5	8	-14
\wedge	Å	Å	\wedge
Ţ	10	<u>و</u>	13

)															
			12-	ſ	0-14	MM					Volts	lts							_
			- 21			_or	V _{IL}	>#	ЧШИ	V _{R1}	V _{R2}	۷.44 ا	V _{th 0}	V _{CEX}	Vcc	V _{ccl}	V _{ccH}		
						16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.5	5.5		
		Pin	-	Test Limits MCBC5401/MCB5401F -55 to +125°C	its CB5401F 25°C				EST CUP	RENT / VO	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:	LIED TO P	INS LIST	ED BEIC	:WC				
Characteristic	Symbol		2	Max	Unit	ة_	V _{II}	-₩	HHI >	V _{R1}	V _{R2}	۲.41	۷#۵	V _{CEX}	V _{cc}	Vcci	Vcch	Gnd	
lnput Forward Current	IF	-	11	-1.6	mAdc	1	1			5	1	1	1		,	i e	4	11*	
Leakage Current	I _{R1}	-		40	μAdc		'	1			,	,	1	1	'	,	4	2,11*	
	\mathbf{I}_{R2}	-		1.0	mAdc	• ;	-	1	1	'	'	,	1	•		,	4	2,11*	
Output Output Voltage	V _{OL}	ñ		0.4	Vdc	e	1	1				1,2			1	4		11*	
Output Leakage Current	ICEX	3		0. 25	mAdc	н 1. 1.				1	1		2	e	1	4	1	11*	
Power Requirements (Total Device) Power Supply Drain	IPDH	4		22	mAdc				1		1,2,6,7,9, 10,12,13	,	1	1	,	-	4	п	
	IPDL	4		8.0	mAdc	1		-	,	1	,					-	4	1,2,11*	
Switching Parameters						Pulse In	Pulse Out												
Turn-On Delay	t pd-	1,3		15**	ns	1	ę	2	1		1	I	•	•	4		1	п	
Turn-Off Delay	t pd+	1,3	à.	45**	ns	1	e	3	1	1	1	1	1	1	4	1	1	П	_
*Ground inputs to gates not under test. **Tested only at 25°C.	es not unde	er test.													1				•

(All Temperatures)

TEST CURRENT/VOLTAGE VALUES