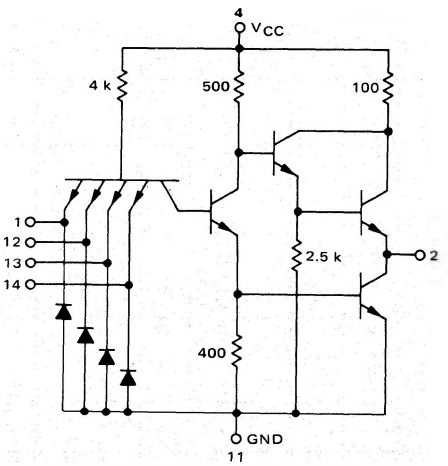
DUAL 4-INPUT "NAND" BUFFER

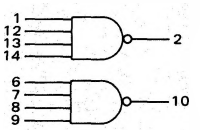
MCBC5440*
MCB5440F*

BEAM LEAD

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gates that are produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic: $2 = \overline{1 \cdot 12 \cdot 13 \cdot 14}$

Negative Logic: $2 = \overline{1 + 12 + 13 + 14}$

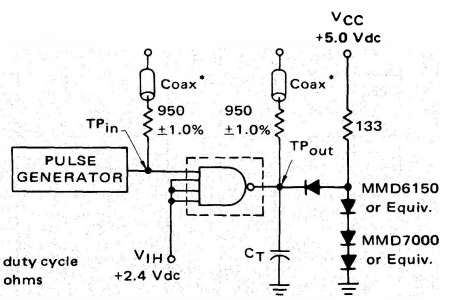
Input Loading Factor = 1

Output Loading Factor = 30

Total Power Dissipation = 50 mW typ/pkg

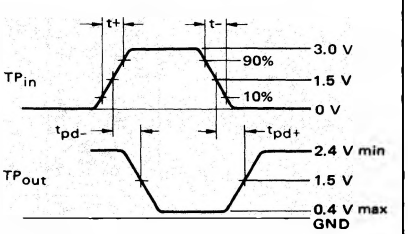
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



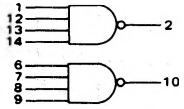
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	Test Limits MCBC5440/MCB5440F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																		
Forward Current	I_F	1	-	-1.6	mAdc	-	-	1	-	-	12,13,14	-	-	-	-	-	4	11*
Leakage Current	I_{R1}	1	-	40	μAdc	-	-	-	1	-	-	-	-	-	-	-	4	11,12,13,14*
	I_{R2}	1	-	1.0	mAdc	-	-	-	-	1	-	-	-	-	-	-	4	11,12,13,14*
Output																		
Output Voltage	V_{OL}	2	-	0.4	Vdc	2	-	-	-	-	-	-	1,12,13,14	-	-	4	-	11*
	V_{OH}	2	2.4	-	Vdc	-	2	-	-	-	12,13,14	-	-	1	-	4	-	11*
Short-Circuit Current	I_{SC}	2	-20	-70	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,11,12,13,14*
Power Requirements (Total Device)																		
Power Supply Drain	I_{PDH}	4	-	27	mAdc	-	-	-	-	-	-	1,6,7,8,9, 12,13,14	-	-	-	-	4	11
	I_{PDL}	4	-	8	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,11,12,13,14*
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,2	-	15**	ns	1	2	-	12,13,14	-	-	-	-	-	4	-	-	11*
Turn-Off Delay	t_{pd+}	1,2	-	22**	ns	1	2	-	12,13,14	-	-	-	-	-	4	-	-	11*

*Ground inputs to gate not under test.
**Tested only at 25°C.