MCF5208PB
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MCF5208 ColdFire® Microprocessor Product Brief

Supports MCF5207 & MCF5208

by: Microcontroller Division

The MCF5207 and MCF5208 devices are highly-integrated 32-bit microprocessors based on the version 2 ColdFire microarchitecture. Both devices contain a 16-Kbyte internal SRAM, an 8-Kbyte configurable cache, a 2-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, a low-power management modeule, and other peripherals that enable the MCF5207 and MCF5208 for use in industrial control and connectivity applications. The MCF5208 device also features a 10/100 Mbps fast ethernet controller.

This document provides an overview of the MCF5207 and MCF5208 microprocessors. It was written from the perspective of the MCF5208 device. See the following section for a summary of differences between the two devices.

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1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

Table 1. MCF5207 & MCF5208 Configurations

Module	MCF5207	MCF5208
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x
Core (System) Clock	up to 166.67 MHz	
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 83.33 MHz	
Performance (Dhrystone/2.1 MIPS)	up to 159	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	16 Kbytes	
SDR/DDR SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	—	x
Low-Power Management Module	x	x
UARTs	3	3
I^2C	x	x
QSPI	x	x
32-bit DMA Timers	4	4
Watchdog Timer (WDT)	x	x
Periodic Interrupt Timers (PIT)	4	4
Edge Port Module (EPORT)	x	x
Interrupt Controllers (INTC)	1	1
16-channel Direct Memory Access (DMA)	x	x
FlexBus External Interface	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE® 1149.1 Test Access Port	x	x
Package	144 LQFP 144 MAPBGA	160 QFP 196 MAPBGA

2 Block Diagram

The MCF5208 superset device is available in a 196-pin mold-array process ball grid array (MAPBGA) or 160-pin quad flat pack (QFP) package. Figure 1 shows a top-level block diagram of the MCF5208.

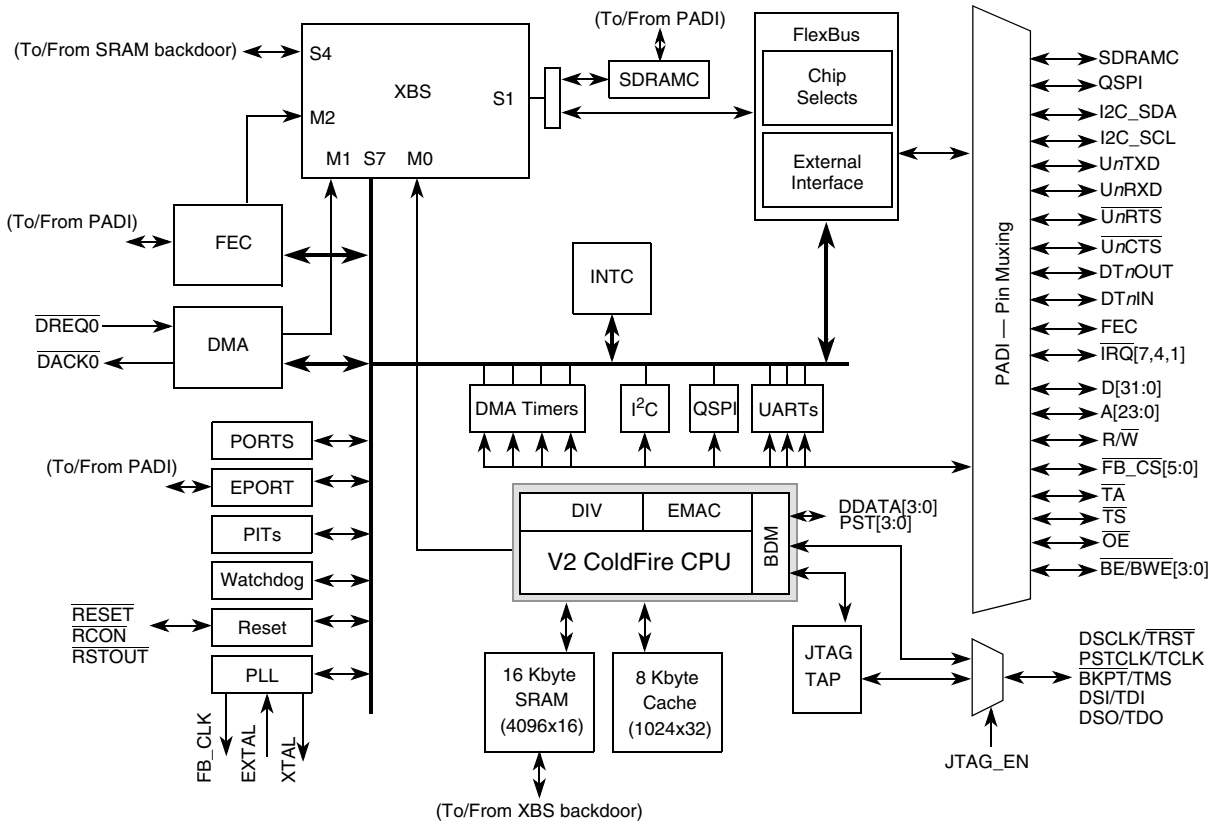

Figure 1. MCF5208 Block Diagram

3 Features

The following is a brief summary of the functional blocks in the MCF5208 superset device. For more details refer to the *MCF5208 ColdFire Microprocessor Reference Manual* (MCF5208RM).

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data path on-chip
  - Processor core runs at twice the bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Implements the ColdFire Instruction Set Architecture, ISA_A+, with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
  - Enhanced multiply-accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
  - Hardware divide execution unit supporting various 32-bit operations
  - Illegal instruction decode that allows for 68K emulation support
- System debug support

  - Background debug mode (BDM) Revision B+ for in-circuit debugging
  - Real time debug support, with nine user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- JTAG support for system level board testing
- On-chip memories
  - 8-Kbyte cache configurable as instruction-only, data-only, or split I-/D-cache
  - 16-Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (e.g., DMA and FEC)
- Power management
  - Fully static operation with processor wait, doze, and stop modes
  - Very rapid response to interrupts from sleep mode
  - Global clock disable register to disable clocks to each peripheral individually
  - Ability to bypass PLL circuitry for low power and low speed (limp) mode to run the device at a fraction of the input clock
- SDR/DDR SDRAM controller
  - Supports a glueless interface to SDR and DDR SDRAM devices
  - 16-bit (DDR) or 32-bit (SDR) fixed memory port width
  - 16 bytes critical word first burst transfer
  - Up to 14 lines of row address, up to 12 (in 32-bit mode) or 13 (in 16-bit mode) column address lines, 2 bits of bank address, and a maximum of two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit mode
  - Supports up to 256 MBytes of memory per chip select, 512 MBytes total
  - Supports page mode to maximize the data rate
  - Supports sleep & self-refresh modes
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII) to external transceiver (PHY)
- Three universal asynchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic
  - DMA support with separate transmit and receive requests
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments

  - Error-detection capabilities
  - Flow control support includes request-to-send ($\overline{\text{U}n\text{RTS}}$) and clear-to-send ($\overline{\text{U}n\text{CTS}}$) lines
- I^2C Module
  - Interchip bus interface for EEPROMs, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only with programmable master bit rates
  - Up to 16 pre-programmed transfers
- Four 32-bit DMA timers
  - 12-ns resolution at 83.33 MHz
  - Programmable prescaler and sources for clock input, including an external clock option
  - Input-capture capability with programmable trigger edge on input pin
  - Output-compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts & DMA trigger capability on input capture or output-compare
- Software watchdog timer
  - 16-bit counter
  - Low power mode support
- Four periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Phase locked loop (PLL)
  - 16 MHz reference frequency
  - Programmable dithering
- Interrupt Controller
  - Support for up to 63 interrupt sources
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA Controller

- 16 fully programmable channels with 32-byte transfer control
- Data movement via dual-address transfers for 8-, 16-, and 32-bit data values
- Programmable source & destination addresses, transfer size, and support for enhanced address modes
- Support for major and minor "nested" counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration
- External request pins for a single channel

- FlexBus (External Interface)
  - Glueless connections to 8-, 16-, or 32-bit external memory devices (SRAM, Flash, ROM, etc.)
  - Support for independent primary and secondary wait states per chip select
  - Programmable address setup & hold time with respect to chip select negation, per transfer direction
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 32-bit bidirectional data bus and 24-bit address bus
  - Up to six chip selects available
  - Byte/write enables (byte strobes)
  - Ability to boot from external memories that are 8, 16, or 32 bits wide
- Chip configuration module (CCM)
  - System configuration during reset
  - Unique part identification number and part revision number
- Reset controller
    - Separate reset in and reset out signals
    - Five reset sources: power-on reset (POR), external, software, watchdog, PLL loss of lock
    - Status flag indication of source of last reset
- General Purpose I/O interface
  - Up to 30 bits of GPIO for the MCF5207
  - Up to 50 bits of GPIO for the MCF5208 (196 MAPBGA)
  - Up to 46 bits of GPIO for the MCF5208 (160 QFP)
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
  - Programmable drive strength or slew rate control for related group of pins

3.1 V2 Core Overview

The processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5208 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands as well as a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

The core also includes a hardware divide unit which performs a number of integer-divide operations. The supported divide functions include: 32-bit dividend and 16-bit divisor producing a 16-bit quotient and a 16-bit remainder, 32-bit dividend and 32-bit divisor producing a 32-bit quotient, and 32-bit dividend and 32-bit divisor producing a 32-bit remainder.

3.2 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access debug information. This allows the processor and system to be debugged without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable registers—a pair of upper and lower address registers, a pair of data registers (a 32-bit data register and a 32-bit data mask register), and four 32-bit PC registers plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor’s supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at one-half the CPU’s clock rate.

3.3 JTAG

The MCF5208 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a bypass register, a boundary-scan register, and

an ID register). The boundary scan register links the device’s pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5208 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample device system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

3.4 On-chip Memories

3.4.1 Cache

The 8-Kbyte cache can be configured into one of three possible organizations: an 8-Kbyte instruction cache, an 8-Kbyte data cache or a split 4-Kbyte instruction/4-Kbyte data cache. The configuration is software-programmable by control bits within the privileged cache configuration register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory, organized as 512 lines, each containing 16 bytes of data. The memories consist of a 512-entry tag array (containing addresses and control bits) and a 8-Kbyte data array, organized as 2048 x 32 bits.

If the desired address is mapped into the cache memory, the output of the data array is driven onto the ColdFire core's local data bus, completing the access in a single cycle. If the data is not mapped into the tag memory, a cache miss occurs and the processor core initiates a 16-byte line-sized fetch. The cache module includes a 16-byte line fill buffer used as temporary storage during miss processing. For all data cache configurations, the memory operates in write-through mode and all operand writes generate an external bus cycle.

3.4.2 SRAM

The SRAM module provides a general-purpose 16-Kbyte memory block that the ColdFire core can access in a single cycle. The memory is ideal for storing critical code or data structures or for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The dual-port SRAM module is also accessible by the DMA and FEC non-core bus masters through the crossbar switch. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a bus-mastering device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

3.5 SDR/DDR SDRAM Controller

The SDRAM controller provides a glueless interface to both SDR and DDR SDRAM memory devices. The module uses a 32-bit (for SDR) or a 16-bit (for DDR) memory port and can address up to 512 MB of data (256 MB per chip select). The controller supports DDR and SDR SDRAM, but both cannot be used at the same time.

3.6 Fast Ethernet Controller (FEC)

The integrated Fast Ethernet Controller (FEC) performs the full set of IEEE® 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media.

3.7 UARTs

The device contains three independent, full-duplex UARTs. The three UARTs can be clocked by the internal bus clock, eliminating the need for an externally supplied clock. They can use DMA requests on transmit-ready and receive-ready as well as interrupt requests for servicing.

3.8 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

3.9 QSPI

The queued serial peripheral interface module provides a high-speed synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, eliminating CPU intervention between transfers.

3.10 DMA Timers (DTIM0-DTIM3)

There are four independent, DMA-transfer-generating 32-bit timers (DTIM[3:0]) on the MCF5208. Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DT*n*IN signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCR*n*). Each of these timers can be configured for input capture or output compare mode. By configuring the internal registers, each timer may be configured to assert an external pin, generate an interrupt on a particular event, or cause a DMA transfer.

3.11 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

3.12 Periodic Interrupt Timers (PIT0-PIT3)

The four periodic interrupt timers (PIT[3:0]) are 16-bit timers that provide precise interrupts at regular intervals with minimal processor intervention. Each timer can either count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

3.13 Clock Module and Phase Locked Loop (PLL)

The MCF5208 contains a 16 MHz crystal oscillator, a phase-locked loop, as well as status and control registers. The PLL's output dividers and dithering waveform are register programmable. The system operates via two main clocks generated by the PLL, typically 166.67 MHz and 83.33 MHz. To improve noise immunity, the PLL has its own power supply inputs, PLL_VDD and PLL_VSS. All other circuits are powered by the normal internal supply pins, VDD and VSS.

The PLL circuitry may be bypassed in order to reduce system speed and therefore decrease power consumption. The external clock (EXTAL) is used directly, with an optional programmable divider, to produce the internal core and bus clocks.

3.14 Interrupt Controller

There is a single interrupt controller on the MCF5208, which can support up to 63 interrupt sources. Each interrupt source has a unique interrupt vector, and all sources of the controller provide a programmable level [1-7].

3.15 DMA Controller

The implementation of the DMA controller is targeted towards cost sensitive applications while providing a high level of functionality. The DMA executes in parallel with the core, enabling transfers of data between the memory and peripherals with little intervention from the core, thus increasing system performance, as well as simplifying software development. The DMA is capable of performing complex data transfers via 16 programmable DMA channels. The hardware microarchitecture includes the DMA engine (which performs source/destination address calculations and data movement operations), and a dedicated memory array containing transfer control descriptors.

3.16 FlexBus External Interface

The FlexBus provides an external interface to 8-, 16-, or 32-bit memory devices (e.g. SRAM, Flash, ROM, etc.). The FlexBus's internal data lines are shared with the SDRAM controller. When the SDRAMC is in DDR mode (DRAMSEL = 1), the D[31:16] signals are dedicated to the SDRAM controller data bus and

the D[15:0] signals are dedicated to the FlexBus data bus. In SDR mode (DRAMSEL = 0) all 32 data lines are shared between the FlexBus and SDRAM controller.

Features are available to support external Flash modules, for secondary wait states on reads and writes and a signal to support active-low address valid ($\overline{TS}$). Six programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

3.17 Reset Controller Module

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. There are five sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- Software

External reset on the $\overline{RSTOUT}$ pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

3.18 GPIO

Unused bus interface and peripheral pins on the device can be used as discrete general-purpose inputs and outputs. These are managed by a dedicated GPIO module that logically groups all pins into ports located within a contiguous block of memory-mapped control registers. Each port has registers that configure, monitor, and control the port pins. Slew rate control or output pad drive strength control is available on all pins.

Most of the pins associated with the FlexBus interface may be used for several different functions. Their primary function is to provide an external interface to access off-chip resources. When not used for this, the pins may be used as general-purpose digital I/O pins.

4 Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

5 Document Revision History

Table 2 provides a revision history for this document.

Table 2. MCF5208PB Document Revision History

Rev. No.	Substantive Change(s)
0	• Initial release

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