

Freescale Semiconductor Reference Manual Addendum

MCF52110RMAD Rev. 2, 12/2011

MCF52110 Reference Manual Addendum

Devices Supported:MCF52110,MCF52100

by: Microcontroller Solutions Group

This document describes corrections to the *MCF52110 Reference Manual*, order number MCF52110RM. For convenience, the addenda items are grouped by revision. Please check our website at

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The current available version of the *MCF52110 Reference Manual* is Revision 2.

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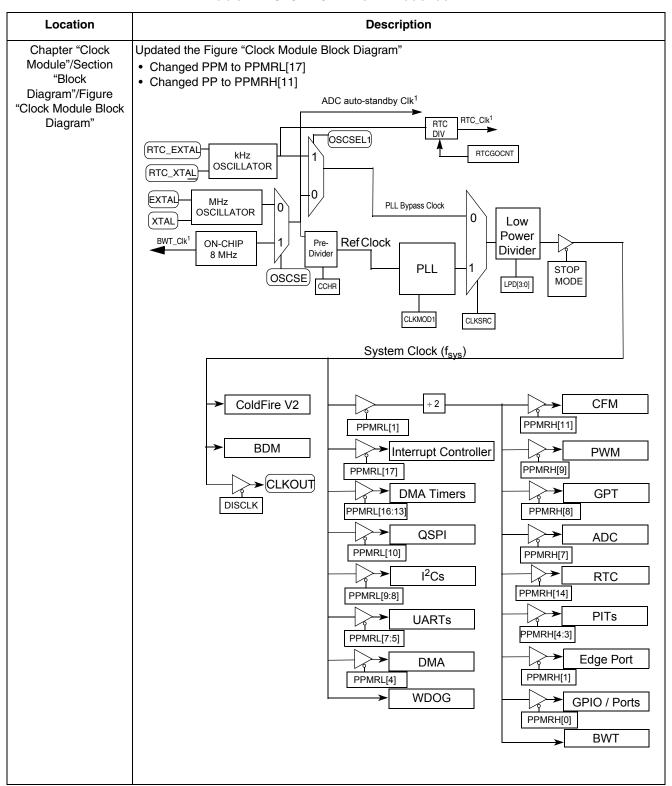




Addendum for Revision 2

1 Addendum for Revision 2

Table 1. MCF52110RM Rev. 2 Addendum



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2 Addendum for Revision 1

Table 2. MCF52110RM Rev. 1 Addendum

Location	Description
Throughout	Formatting, layout, spelling, and grammar corrections.
Table 2-1 / Page 2-3	Synchronized the table in the reference manual and the device data sheet.
Table 6-4 / Page 6-6	Corrected the CCHR reset value (was 0x04, is 0x00).
Figure 6-6 / Page 6-12	Added the missing last digit (0) to the CCHR reset value.
Figure 6-12 / Page 6-19	Deleted the RS resistor.
Chapter 8	Deleted references to nonexistent FlexCAN module.
Chapter 11	Added information about the RTC general oscillator count registers, RTCGOCU and RTCGOCL.
Figure 11-13	Corrected the code example for initializing the RTC.
Section 12.5.4 / Page 12-7	Updated the section to reflect the fact that the CWT does not cause a hardware reset.
Table 12-6 / Page 12-8	In the CWCR[CWRI] field description, changed "The interrupt level for the CWT is programmed in the interrupt control register 7 (ICR7)" to "The interrupt level for the CWT is programmed in the interrupt control register 8 (ICR8)".
Table 12-15 / Page 12-18	Deleted reference to nonexistent FlexCAN module.
Section 12.7.3.1 / Page 12-14	 Rewrote the introductory text describing the MPR (removing erroneous reference to a fast Ethernet controller). Corrected the MPR reset value (was 0x11, is 0x1).
Section 14-1 / Page 14-2	Deleted the sentence beginning with "For many peripheral devices".
Table 14-2 / Page 14-5	Deleted the entry for the (nonexistent) GSWIACK register.
Section 14.3.8 / Page 14-16	Deleted references to the (nonexistent) GSWIACK register.
Section 16.4 / Page 16-12	Deleted the sentence "BCR n decrements when an address transfer write completes for a single-address access (DCR n [SAA] = 0), or when SAA equals 1."
Figure 23-6 / Page 23-9	Added a note to clarify the UCSRn reset values.
Figure 23-20 / Page 23-21	 Corrected the label of the top signal (was UnTXD, is UnRXD). Corrected the text in the footnote (was TXRTS, is RXRTS).
Figure 23-23 / Page 23-24	Corrected the UnTXD label (was "Input", is "Output").
Figure 23-24 / Page 23-25	 Corrected a label on the bottom row (was UMR1n[PT]=2, is UMR1n[PT]=1). Deleted duplicate UMR1n[PM]=11 label.
Section 23.5.1.2 / Page 23-27	Added example DMA configuration steps.
Section 26.3.2.5.1 / Page 26-18	Corrected the numerical values in the left-aligned example.
Section 26.3.2.6.1 / Page 26-20	Corrected the numerical values in the center-aligned example.
Appendix A	 Deleted the entry for the (nonexistent) GSWIACK register. Added entries for the RTCGOCU and RTCGOCL registers.

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Revision History

3 Revision History

Table 3 provides a revision history for this document.

Table 3. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1	Initial release, incorporating corrections listed in Table 2.	06/2007
2	Corrected errors in Chapter "Clock Module" listed in Table 1	12/2011



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Document Number: MCF52110RMAD

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