

ColdFire® Embedded Controllers

MCF521xx

Fact Sheet

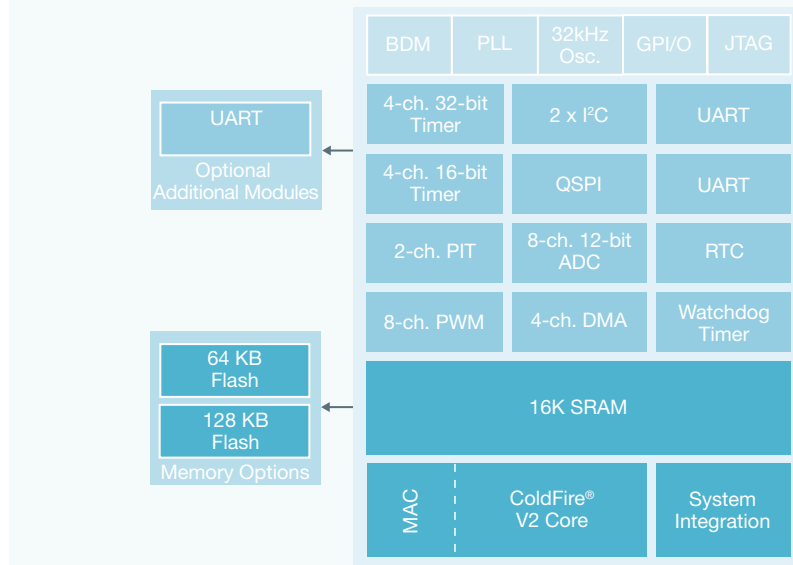
Overview

The MCF521xx family of embedded controllers expands the ColdFire® device portfolio by bringing a highly integrated and diverse feature set to low cost, low power microcontrollers (MCUs). Based on the Version 2 ColdFire core, the MCF521xx MCUs are ideal for power-conscious designers who want the performance and flexibility of a 32-bit microcontroller plus a rich set of on-chip peripherals at a low cost.

Operating at a frequency up to 80 MHz out of flash memory, the MCF521xx family features 16 Kbytes of internal static random access memory (SRAM) and up to 128 Kbytes of flash memory, an 8-channel, 12-bit analog-to-digital converter (ADC), four 32-bit timers with DMA request capability and a 4-channel DMA controller.

The communications peripherals enable easy connection to other systems. Up to three universal asynchronous receiver/transmitters (UARTs) provide medium to long distance communication to other control systems or computers. Two inter-integrated circuit (I²C) modules and a queued serial peripheral interface (QSPI) allow in-system communication to connected peripherals.

These devices are specifically crafted for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

MCF521xx Block Diagram


| Features | Benefits |
|---|--|
| 32-Bit V2 ColdFire Central Processing Unit (CPU) | |
| 80-MHz / 3.3V CPU | Offers high performance at low voltage levels for battery-operated 32-bit applications |
| Temperature range of -40°C to 85°C | Allows for application development in the demanding industrial market |
| Support for up to 127 interrupt sources with priority and level encoding | Allows for exceptional software flexibility and optimization for real-time applications |
| Multiply-Accumulate (MAC) unit with 32-bit accumulator to support 16x16 or 32x32 operations | Provides hardware acceleration of multiply and divide instructions improving overall system performance |
| On-Chip Memory | |
| Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses | Allows user to take full advantage of in-application, re-programmability benefits in virtually any environment |
| 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support | Allows write access from the DMA and CPU simultaneously, freeing the CPU resource quickly |
| Power Management | |
| Reduced power wait mode | Allows for analog sampling in a reduced power state |
| Internal relaxation oscillator — internal clock source | Eliminates the use of an external clock source which ultimately reduces the system costs |
| Oscillator (OSC) — Loop-control Pierce oscillator; Fundamental mode Crystal or ceramic resonator | Improves communications peripheral timing accuracy |

| Features Cont. | Benefits Cont. |
|--|---|
| Peripherals | |
| Battery backed Real Time Clock (RTC) with 32 KHz Oscillator | Adds time of day and calendar functionality to system even while main power is removed from MCU. |
| Fast Analog to Digital Converter (ADC) 12-bit resolution; 1.125 μ s conversion time; automatic compare function and offset correction | Eight channels allows up to eight analog devices to be sampled at extremely high speeds with quick conversion times. Dual converters allow differential measuring and increase conversion speed |
| Serial communications interface (UART) modules offering asynchronous communications, 13-bit break option, flexible baud rate generator, double buffered transmit and receive and optional H/W parity checking and generation | Provides full duplex asynchronous/synchronous receiver and transmitter deriving an operating frequency from the internal bus clock or external clock using the timer pin |
| Serial peripheral interfaces (QSPI) with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting | Allows full-duplex, asynchronous, NRZ serial communication between MCU and remote devices. Queued SPI provides messaging automation and buffering of messages |
| Two I ² C modules; Up to 400 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing | Two I ² C ports enable use of the external OTG interface, while having an additional expansion channel available that can be used by an LCD controller or IIC EEPROM, for example. This provides high bandwidth and ease of connectivity |
| Timer (TIM)—One 4-channel; selectable input capture, output compare on each channel | Generates output waveforms and timer software delays. These functions allow simultaneous input waveform measurements and output waveform generation |
| Pulse-Width Modulation (PWM) - 8 channel module with PCM control | New PCM function eases external filter requirements |
| Two Programmable Interrupt Timer Modules (PIT) | Allows two programmable periodic interrupts to system. The second timer allows system application to have their own timer while scheduler or OS has its own |
| DMA Controller with 4 fully programmable channels | Enables fast transfers of data with minimal processor interaction |
| Input/Output | |
| 56 general purpose input/output (GPIO)s and one input-only and one output only pin | Results in a large number of flexible I/O pins that allow vendors to easily interface the device into their own designs |
| System Protection | |
| Secondary Watchdog Timer (SWT) Module | Allows the device to recognize run-away code and resets the processor to avoid lock-up states |
| Low-voltage detection with reset or interrupt | Alarms the system of voltage drops outside of the typical operating range |
| Flash block protection | Helps to prevent unauthorized access to flash RAM which greatly reduces the chance of losing vital system code |
| Development Support | |
| Real-time Trace Support | A fundamental debug function that defines the dynamic execution path |
| Background Debug Module (BDM) | Single wire interface for both programming and debugging that allows developers to use the same interface for multiple platforms |
| Breakpoint capability | Allows six breakpoints (4 PC, 1 address, and 1 data) that can be configured into one or two level trigger |

Target Applications

- HVAC building and control systems
- Medical instrumentation and monitors
- Fire/security control and monitoring systems
- Factory and automation systems
- Measurement equipment
- Hand-held medical/industrial applications
- Lighting control
- Industrial instrumentation
- Consumer electronics
- Low power industrial applications

Cost Effective Development Tools

M52211EVB

US\$299 MSRP

Full-featured evaluation system for both the MCF5221x and the MCF521xx device families.

CodeWarrior® Development Studio for Microcontrollers 6.4

Complimentary

CodeWarrior Development Studio for Microcontrollers is a single tool suite that supports software development for Freescale's ColdFire 32-bit microcontrollers and microprocessors.

Package Options

| Part Number | Temp. Range | Package |
|---------------|---------------|-----------|
| MCF52100CAE66 | -40°C to 85°C | 64 QFP |
| MCF52100CEP66 | -40°C to 85°C | 64 QFN |
| MCF52100CVM66 | -40°C to 85°C | 81 MAPBGA |
| MCF52100CVM80 | -40°C to 85°C | 81 MAPBGA |
| MCF52110CAE66 | -40°C to 85°C | 64 QFP |
| MCF52110CEP66 | -40°C to 85°C | 64 QFN |
| MCF52110CVM66 | -40°C to 85°C | 81 MAPBGA |
| MCF52110CVM80 | -40°C to 85°C | 81 MAPBGA |
| MCF52110CAF80 | -40°C to 85°C | 100 LQFP |

Learn More:

For more information about ColdFire family products, please visit www.freescale.com/coldfire.