MCF52235 ColdFire® Integrated Microcontroller Product Brief

This document provides an overview of the major features and functional components of the MCF52235 family of microcontrollers. The MCF52235 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microcontrollers that also includes the MCF52230, MCF52231, MCF52232, MCF52233, MCF52234, and MCF52236. Table 1 summarizes the differences between these parts. This document is written from the perspective of the MCF52235.

The MCF52235 represents a family of highly-integrated 32-bit microcontrollers based on the V2 ColdFire microarchitecture operating at a core/bus frequency up to 60 MHz. On-chip memories connected tightly to the processor core include up to 256 Kbytes of flash and 32 Kbytes of static random access memory (SRAM). On-chip modules include:

- V2 ColdFire core providing 56 Dhrystone 2.1 MIPS @ 60 MHz executing out of on-chip flash memory using enhanced multiply accumulator (EMAC) and hardware divider

- Enhanced Multiply Accumulate Unit (EMAC) and hardware divide module

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- Cryptographic Acceleration Unit (CAU) coprocessor
- Fast Ethernet Controller (FEC)
- On-chip Ethernet Transceiver (PHY)
- FlexCAN controller area network (CAN) module
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)
- Inter-integrated circuit (I²C™) bus controller
- Queued serial peripheral interface (QSPI) module
- Eight-channel 12-bit fast analog-to-digital converter (ADC)
- Four channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support (DTIM)
- Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM) and pulse accumulation
- Eight/Four-channel 8/16-bit pulse width modulation timers (two adjacent 8-bit PWMs can be concatenated to form a single 16-bit timer)
- Two 16-bit periodic interrupt timers (PITs)
- Real-time clock (RTC) module
- Programmable software watchdog timer
- Two interrupt controllers providing every peripheral with a unique selectable-priority interrupt vector plus seven external interrupts with fixed levels/priorities
- Clock module with on-chip oscillator and integrated phase locked loop (PLL)
- Test access/debug port (JTAG, BDM)

1   MCF52235 Family Configurations

Table 1. MCF52235 Family Configurations

Module	52230	52231	52232	52233	52234	52235	52236
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•	•
System Clock (MHz)	60	60	50	60	60	60	50
Performance (Dhrystone 2.1 MIPS)	56	56	46	56	56	56	46
Flash / Static RAM (SRAM)	128/32 Kbytes	128/32 Kbytes	128/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes
Interrupt Controllers (INTC0/INTC1)	•	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•	•
Random Number Generator and Crypto Acceleration Unit (CAU)	—	—	—	—	—	•	—
FlexCAN 2.0B Module	—	•	—	—	•	•	—

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Table 1. MCF52235 Family Configurations (continued)

Module	52230	52231	52232	52233	52234	52235	52236
Fast Ethernet Controller (FEC) with on-chip interface (EPHY)	•	•	•	•	•	•	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•	•
Programmable Interrupt Timer	2	2	2	2	2	2	2
Four-Channel General Purpose Timer	•	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4	4
QSPI	•	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port[1]	•	•	•	•	•	•	•
Package	80 LQFP 112 LQFP	80 LQFP 112 LQFP	80 LQFP	80 LQFP 112 LQFP	112 LQFP 121 MAPBGA	112 LQFP 121 MAPBGA	80 LQFP

NOTES:
[1] The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

2 Block Diagram

The MCF52235 comes in 80- and 112-pin low-profile quad flat pack (LQFP) and 121-pin MAPBGA packages operating in single-chip mode only. Figure 1 shows a top-level block diagram of the MCF52235.
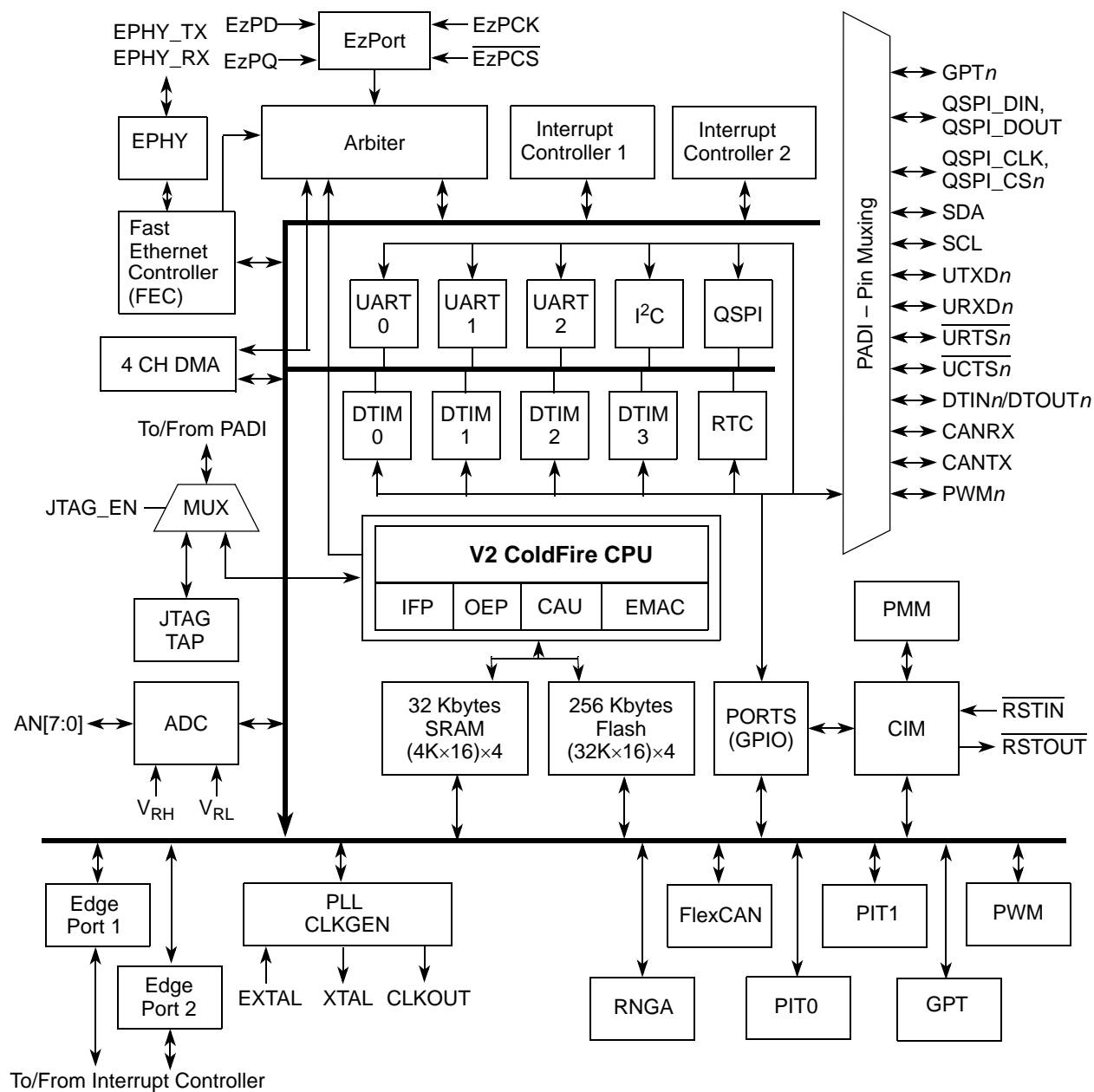
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Figure 1. MCF52235 Block Diagram

3 Features

This document contains information on a new product under development. Freescale reserves the right to change or discontinue this product without notice. Specifications and information herein are subject to change without notice.

3.1 Feature Overview

The MCF52235 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 60 MHz processor core frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
  - Cryptography Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - FIPS-140 compliant random number generator
  - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - Up to 32 Kbytes of dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 256 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- Fast Ethernet Controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- On-chip Ethernet Transceiver (EPHY)

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- — Digital adaptive equalization
- — Supports auto-negotiation
- — Baseline wander correction
- — Full-/Half-duplex support in all modes
- — Loopback modes
- — Supports MDIO preamble suppression
- — Jumbo packet
- FlexCAN 2.0B module
  - — Based on and includes all existing features of the Freescale TouCAN module
  - — Full implementation of the CAN protocol specification version 2.0B
    - – Standard Data and Remote Frames (up to 109 bits long)
    - – Extended Data and Remote Frames (up to 127 bits long)
    - – 0–8 bytes data length
    - – Programmable bit rate up to 1 Mbit/sec
  - — Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - — Unused Message Buffer space can be used as general purpose RAM space
  - — Listen only mode capability
  - — Content-related addressing
  - — No read/write semaphores required
  - — Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - — Programmable transmit-first scheme: lowest ID or lowest buffer number
  - — Time stamp based on 16-bit free-running timer
  - — Global network time, synchronized by a specific message
  - — Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - — 16-bit divider for clock generation
  - — Interrupt control logic with maskable interrupts
  - — DMA support
  - — Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - — Up to 2 stop bits in 1/16 increments
  - — Error-detection capabilities
  - — Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - — Transmit and receive FIFO buffers
- I²C module

- — Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- — Fully compatible with industry-standard I²C bus
- — Master and slave modes support multiple masters
- — Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - — Full-duplex, three-wire synchronous transfers
  - — Up to four chip selects available
  - — Master mode operation only
  - — Programmable bit rates up to half the CPU clock frequency
  - — Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - — Eight analog input channels
  - — 12-bit resolution
  - — Minimum 1.125 µs conversion time
  - — Simultaneous sampling of two channels for motor control applications
  - — Single-scan or continuous operation
  - — Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - — Unused analog channels can be used as digital I/O
- Four 32-bit DMA timers
  - — 17-ns resolution at 60 MHz
  - — Programmable sources for clock input, including an external clock option
  - — Programmable prescaler
  - — Input capture capability with programmable trigger edge on input pin
  - — Output compare with programmable mode for the output pin
  - — Free run and restart modes
  - — Maskable interrupts on input capture or output compare
  - — DMA trigger capability on input capture or output compare
- Four-channel general purpose timers
  - — 16-bit architecture
  - — Programmable prescaler
  - — Output pulse widths variable from microseconds to seconds
  - — Single 16-bit input pulse accumulator
  - — Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - — One dual-mode pulse accumulation channel

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- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - 25 MHz crystal input
  - On-chip PLL can generate core frequencies up to maximum 60MHz operating frequency
  - Provides clock for integrated EPHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers

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- — Source/destination address pointers that can increment or remain constant
- — 24-bit byte transfer counter per channel
- — Auto-alignment transfers supported for efficient block movement
- — Bursting and cycle steal support
- — Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - — Separate reset in and reset out signals
  - — Seven sources of reset:
    - – Power-on reset (POR)
    - – External
    - – Software
    - – Watchdog
    - – Loss of clock
    - – Loss of lock
    - – Low-voltage detection (LVD)
  - — Status flag indication of source of last reset
- Chip integration module (CIM)
  - — System configuration during reset
  - — Selects one of three clock modes
  - — Configures output pad drive strength
  - — Unique part identification number and part revision number
- General purpose I/O interface
  - — Up to 56 bits of general purpose I/O
  - — Bit manipulation supported via set/clear functions
  - — Programmable drive strengths
  - — Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

3.2 Feature Details

3.2.1 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline

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stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 16×16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

3.2.2   Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, access debug information and real-time tracing capability is provided on 112-and 121-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF52235 implements revision B+ of the ColdFire Debug Architecture.

The MCF52235's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF52235 includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 112 and 121-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

3.2.3   JTAG

The MCF52235 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF52235 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF52235 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF52235 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

3.2.4 On-Chip Memories

3.2.4.1 SRAM

The dual-ported SRAM module provides a general-purpose 16- or 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16- or 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

3.2.4.2 Flash

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32 K×16-bit flash arrays to generate 256 Kbytes of 32-bit flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle flash arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash programming interface that allows the flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips. This allows easy device programming via Automated Test Equipment or bulk programming tools.

3.2.5 Cryptography Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions,

specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

3.2.6 Power Management

The MCF52235 incorporates several low-power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

3.2.7 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

3.2.8 UARTs

The MCF52235 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

3.2.9 I^{2}C Bus

The I^{2}C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices on a circuit board.

3.2.10 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

3.2.11 Fast ADC

The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 10- or 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

3.2.12 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the each device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

3.2.13 General Purpose Timer (GPT)

The general purpose timer (GPT) is a 4-channel timer module consisting of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

3.2.14 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or can be a free-running down-counter.

3.2.15 Pulse Width Modulation (PWM) Timers

The MCF52235 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0 to 100%. The PWM outputs have programmable polarity and can be programmed as left-aligned outputs or center-aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a

single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

3.2.16 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

3.2.17 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

3.2.18 Interrupt Controller (INTC0/INTC1)

There are two interrupt controllers on the MCF52235. These interrupt controllers are organized as seven levels with up to nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and provide each peripheral with all necessary interrupts. Each internal interrupt has a programmable level [1-7] and priority within the level. The seven external interrupts have fixed levels/priorities.

3.2.19 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the occurrence of certain UART or DMA timer events.

3.2.20 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

3.2.21 GPIO

Nearly all pins on the MCF52235 have general purpose I/O capability in addition to their primary functions and are grouped into 8-bit ports. Some ports do not utilize all 8 bits. Each port has registers that configure, monitor, and control the port pins.

4 Part Numbers and Packaging

Table 2. Orderable Part Number Summary

Freescale Part Number	Description	Speed (MHz)	Flash/SRAM (Kbytes)	Package	Temp range (°C)
MCF52230CAF60	MCF52230 Microcontroller	60	128 / 32	80 LQFP	-40 to +85
MCF52230CAL60	MCF52230 Microcontroller	60	128 / 32	112 LQFP	-40 to +85
MCF52231CAF60	MCF52231 Microcontroller, FlexCAN	60	128 / 32	80 LQFP	-40 to +85
MCF52231CAL60	MCF52231 Microcontroller, FlexCAN	60	128 / 32	112 LQFP	-40 to +85
MCF52232CAF50	MCF52232 Microcontroller	50	128 / 32	80 LQFP	-40 to +85
MCF52232AF50	MCF52232 Microcontroller	50	128 / 32	80 LQFP	0 to +70
MCF52233CAF60	MCF52233 Microcontroller	60	256 / 32	80 LQFP	-40 to +85
MCF52233CAL60	MCF52233 Microcontroller	60	256 / 32	112 LQFP	-40 to +85
MCF52234CAL60	MCF52234 Microcontroller, FlexCAN	60	256 / 32	112 LQFP	-40 to +85
MCF52234CVM60	MCF52234 Microcontroller, FlexCAN	60	256 / 32	121 MAPBGA	-40 to +85
MCF52235CAL60	MCF52235 Microcontroller, FlexCAN, CAU, RNGA	60	256 / 32	112 LQFP	-40 to +85
MCF52235CVM60	MCF52235 Microcontroller, FlexCAN, CAU, RNGA	60	256 / 32	121 MAPBGA	-40 to +85
MCF52236CAF50	MCF52236 Microcontroller	50	256 / 32	80 LQFP	-40 to +85
MCF52236AF50	MCF52236 Microcontroller	50	256 / 32	80 LQFP	0 to +70

5　Revision History

Table 3. Revision History

Revision	Description
0	Initial release.
1	• Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added family configuration section and table. • Added information for the MCF52230 and MCF52234 parts. • Deleted information for nonexistent MCF52232 part. • Added revision history.
2	• Formatting, layout, spelling, and grammar corrections. • Revised introductory section. • Added information for the new MCF52232 and MCF52236 parts.

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