MCF52277PB
Rev. 1, 2/2009

MCF5227*x* ColdFire® Microprocessor Product Brief

Supports MCF52274 & MCF52277

by: Microcontroller Solutions Group

The MCF5227*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 2 ColdFire microarchitecture. All MCF5227*x* devices contain a 128-Kbyte internal SRAM, LCD and touchscreen controllers, a USB On-the-Go interface, a 2-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, a serial boot facility, CAN module, a SSI interface, up to three UARTs, an SPI, and other peripherals that enable the MCF5227*x* family for use in general purpose industrial control applications.

This document provides an overview of the MCF5227*x* microprocessor family, focusing on its highly diverse feature set. It was written from the perspective of the MCF52277 device. However, it also pertains to the MCF52274. See the following section for a summary of differences between the devices of the MCF5227*x* family.

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1 Application Examples

The MCF5227*x* family is well suited for human interface applications that require a broad range of peripherals and high performance to enable competitive and cost-effective system solutions. As shown in the following examples, this microprocessor is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

1.1 Operator Interface

Figure 1 shows the MCF52277 used in a typical operator interface application.

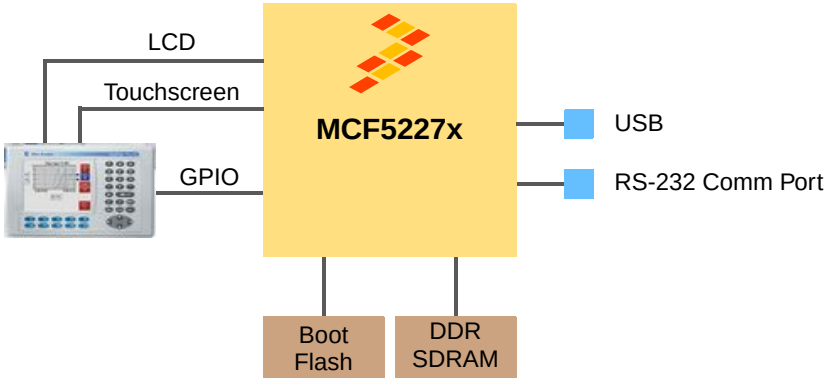


Figure 1. Operator Interface Application Example

2 Features

2.1 MCF5227*x* Family Comparison

The following table compares the various device derivatives available within the MCF5227*x* family.

Table 1. MCF5227*x* Family Configurations

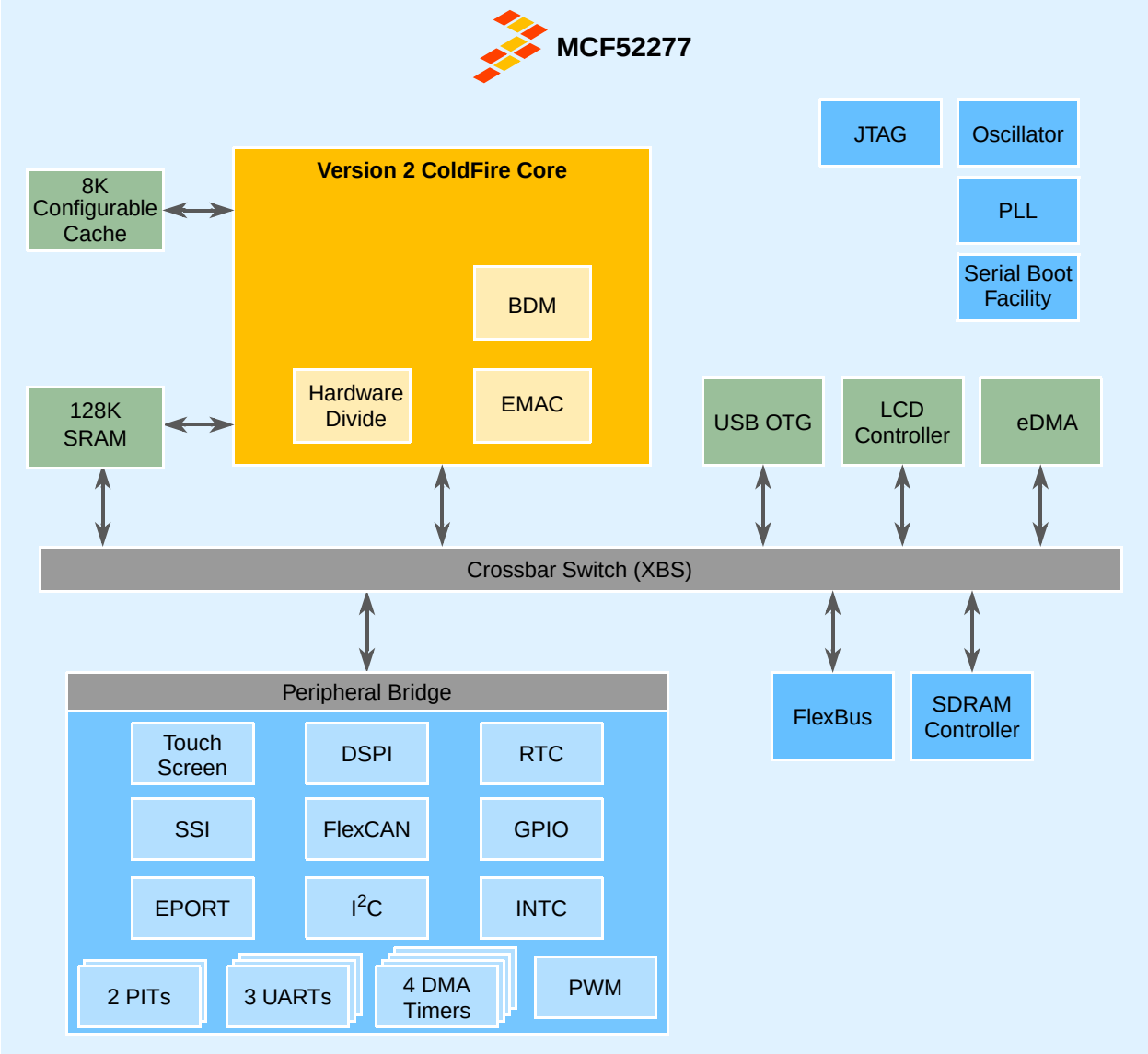
Module	MCF52274	MCF52277
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 120 MHz	up to 166.67 MHz
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 60 MHz	up to 83.33 MHz
Performance (Dhrystone/2.1 MIPS)	up to 114	up to 159
Static RAM (SRAM)	128 Kbytes	
Configurable Cache	8 Kbytes	
ASP Touchscreen Controller	•	•
LCD Controller	12-bit color	18-bit color

Table 1. MCF5227*x* Family Configurations (continued)

Module	MCF52274	MCF52277
USB 2.0 On-the-Go	•	•
FlexBus External Interface	•	•
SDR/DDR SDRAM Controller	•	•
FlexCAN 2.0B communication module	•	•
Real Time Clock	•	•
Watchdog Timer	•	•
16-channel Direct Memory Access (DMA)	•	•
Interrupt Controllers (INTC)	1	1
Synchronous Serial Interface (SSI)	•	•
I^2C	•	•
DSPI	•	•
UARTs	3	3
32-bit DMA Timers	4	4
Periodic Interrupt Timers (PIT)	2	2
PWM Module	•	•
Edge Port Module (EPORT)	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	176 LQFP	196 MAPBGA

2.2 Block Diagram

Figure 2 shows a top-level block diagram of the MCF52277 superset device.



LEGEND

BDM	– Background debug module	**LCD**	– Liquid-crystal display
DSPI	– DMA serial peripheral interface	**PIT**	– Programmable interrupt timer
eDMA	– Enhanced direct memory access	**PLL**	– Phase-locked loop module
EMAC	– Enchanced multiply-accumulate unit	**PWM**	– Pulse-width modulator
EPORT	– Edge port module	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-intergrated circuit	**UART**	– Universal asynchronous receiver/transmitter
INTC	– Interrupt controller	**USB OTG**	– Universal Serial Bus On-the-Go controller
JTAG	– Joint Test Action Group interface		

Figure 2. MCF52277 Block Diagram

2.3 Operating Parameters

- -40ºC to 85ºC junction temperature devices are available
- 1.5V Core, 3.3V I/O, 1.8V/2.5V/3.3V external memory bus

2.4 Packages

Depending on device, the MCF5227*x* family is available in the following packages:

- 176-pin low-profile quad flat pack (LQFP)
- 196-pin molded array process ball grid array (MAPBGA)

2.5 Chip Level Features

- Version 2 ColdFire® Core with EMAC
- Up to 159 Dhrystone 2.1 MIPS @ 166.67 MHz
- 8 Kbytes configurable cache (instruction only, data only, or split instruction/data)
- 128 Kbytes internal SRAM
- Support for booting from SPI-compatible flash, EEPROM, and FRAM devices
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 16 channel DMA controller
- 16- or 32-bit SDR/DDR controller
- USB 2.0 On-the-Go controller
- Liquid crystal display controller
- Touchscreen controller
- FlexCAN module
- 4 32-bit timers with DMA support
- DMA supported serial peripheral interface (DSPI)
- 3 UARTs
- I^2C bus interface
- Synchronous serial interface (SSI)
- Plus-width modulator (PWM)
- Real-time clock (RTC)
- Two programmable interrupt controllers (PIT)

2.6 Module-by-Module Feature List

The following is a brief summary of the functional blocks in the MCF52277 superset device. For more details refer to the *MCF52277 ColdFire Microprocessor Reference Manual* (MCF52277RM).

2.6.1 Version 2 ColdFire Variable-Length RISC Processor

- Static operation
- 32-bit address and data path on-chip
- Maximum 166.67 MHz processor core and 83.33 MHz bus frequency
- Sixteen total general-purpose 32-bit registers data and address
- Enhanced multiply-accumulate unit (EMAC) for DSP and fast multiply operations
- Hardware divide execution unit supporting various 32-bit operations
- Implements the ColdFire Instruction Set Architecture, ISA_A+

2.6.2 On-chip Memories

- 128 Kbyte dual-ported SRAM on CPU internal bus
  - Accessible to non-core bus masters (e.g. DMA, USB OTG, and LCD controller) via the crossbar switch
- 8 Kbyte cache, configurable as instruction-only, data-only, or split I-/D-cache

2.6.3 Phase Locked Loop (PLL)

- 16–40 MHz reference crystal
- Loss-of-lock detection

2.6.4 Power Management

- Fully static operation with processor sleep and whole chip stop modes
- Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Peripheral power management register to enable/disable clocks to most modules
- Software controlled disable of external clock input for low power consumption

2.6.5 Chip Configuration Module (CCM)

- System configuration during reset
- Bus monitor
- Configurable output pad drive strength control
- Unique part identification and part revision numbers
- Serial boot capability
  - Supports SPI-compatible EEPROM, flash, and FRAM
  - Configurable boot clock frequency

2.6.6 Reset Controller

- Separate reset in and reset out signals
- Six sources of reset: power-on reset (POR), external, software, watchdog timer, loss of lock, JTAG instruction
- Status flag indication of source of last reset

2.6.7 System Control Module

- Access control registers
- Core watchdog timer with a 2^n (where n = 8–31) clock cycle selectable timeout period
- Core fault reporting

2.6.8 Crossbar Switch Module

- Concurrent access from different masters to different slaves
- Slave arbitration attributes configured on a slave by slave basis
- Fixed or round-robin arbitration

2.6.9 Liquid Crystal Display Controller (LCDC)

- Support for single (non-split) screen monochrome/color LCD panels and self-refresh type LCD panels
- 16 simultaneous gray-scale levels from a palette of 16 for monochrome display
- Maximum supported panel size of 600 × 800 pixels
- 4(mapped to RGB444)/8(RGB444)/12 bits per pixel (bpp) for passive color panel
- 4(mapped to RGB666)/8(mapped to RGB666)/12(RGB444)/16(RGB565)/18 bpp for TFT

2.6.10 Touchscreen Controller

- 12-bit 125 kS/s ADC for touchscreen
- Ratiometric measurements
- Touch/pressure measurements
- Supports 4/5/7 and 8-wire touchscreen configurations
- Supports automatic sampling, single-round sampling, and manual sampling modes
- Provides data-ready and FIFO-full interrupts
- Pen-down detection circuitry to generate pen interrupt request
- True differential input
- Built-in selectable reference generator
- Support for temperature compensation by software

- Power-down capability
- 1.5/3.3 V dual power supply
- Internal or external reference
- Conversion executed synchronously to bus clock
- Triggerable through software and/or external hardware

2.6.11 Universal Serial Bus (USB) 2.0 On-The-Go (OTG) Controller

- Support for full speed (FS) and low speed (LS) via an on-chip FS/LS transceiver
- Uses 60 MHz reference clock based off of the system clock or from an external pin

2.6.12 SDR/DDR SDRAM Controller

- Supports a glueless interface to SDR and DDR SDRAM devices
- Support for 16- or 32-bit fixed memory port width for SDR SDRAM devices; 16-bit fixed memory port width for DDR SDRAM devices.
- 16-byte critical word first burst transfer
- Up to 13 lines of row address, up to 12 (32-bit bus) or 13 (16-bit bus) column address lines, 2 bits of bank address, and two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit bus mode.
- Supports up to 512 MByte of memory; minimum memory configuration of 8 MByte
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode
- Shares address and data bus with the FlexBus interface

2.6.13 FlexBus (External Interface)

- Glueless connections to 8-, 16-, and 32-bit external memory devices (SRAM, flash, ROM, etc.)
- Support for independent primary and secondary wait states per chip select
- Programmable address setup and hold time with respect to chip-select assertion, per transfer direction
- Glueless interface to SRAM devices with or without byte strobe inputs
- Programmable wait state generator
- 32-bit external bidirectional data bus and 24-bit address bus
- Up to six chip selects available
- Byte/write enables (byte strobes)
- Ability to boot from external memories that are 8, 16, or 32 bits wide
- Shares address and data bus with the SDRAM controller

2.6.14 Synchronous Serial Interface (SSI)

- Supports shared (synchronous) transmit and receive sections
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Gated clock mode operation requiring no frame sync
- Programmable data interface modes such as I^2S, LSB aligned, and MSB aligned
- Programmable word length up to 24 bits
- AC97 support

2.6.15 FlexCAN Module

- Full implementation of the CAN protocol specification version 2.0B
  - Standard data and remote frames (up to 109 bits long)
  - Extended data and remote frames (up to 127 bits long)
  - 0–8 bytes data length
  - Programmable bit rate up to 1 Mbit/sec
- Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Unused MB space can be used as general purpose RAM space
- Listen-only mode capability
- Content-related addressing
- Three programmable mask registers: global (for MBs 0-13), special for MB14 and special for MB15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message

2.6.16 Real-Time Clock

- Full clock: days, hours, minutes, seconds
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
- Operation determined by reference input oscillator clock frequency and value programmed into user-accessible registers
- Ability to wake the processor from low-power modes (wait, doze, and stop) via the RTC interrupts

2.6.17 Programmable Interrupt Timers (PIT)

- Two programmable interrupt timers each with a 16-bit counter
- Configurable as a down counter or free-running counter

2.6.18 DMA Timers

- Four 32-bit timers with DMA and interrupt request trigger capability
- Input capture and reference compare modes

2.6.19 DMA Serial Peripheral Interface (DSPI)

- Full-duplex, three-wire synchronous transfer
- Up to three chip selects available
- Master and slave modes with programmable master bit-rates
- Up to 16 pre-programmed transfers

2.6.20 Pulse Width Modulation (PWM) Module

- Four independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel

2.6.21 Universal Asynchronous Receiver Transmitters (UARTs)

- 16-bit divider for clock generation
- Interrupt control logic
- DMA support with separate transmit and receive requests
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to 2 stop bits in 1/16 increments
- Error-detection capabilities

2.6.22 I^2C Module

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- Fully compatible with industry-standard I^2C bus
- Master or slave modes support multiple masters
- Automatic interrupt generation with programmable level

2.6.23 Interrupt Controllers

- Two interrupt controllers, supporting up to 64 interrupt sources each, organized as seven programmable levels
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source plus a global mask-all capability
- Support for service routine software interrupt acknowledge (IACK) cycles
- Combinational path to provide wake-up from low power modes

2.6.24 Edge Port Module

- Each pin can be individually configured as low level sensistive interrupt pin or edge-detecting interrupt pin (rising, falling, or both)
- Exit stop mode via level-detect function

2.6.25 DMA Controller

- 16 fully programmable channels with 32-byte transfer control
- Data movement via dual-address transfers for 8-, 16-, 32- and 128-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration
- External request pins for one channel

2.6.26 General Purpose I/O interface

- Up to 47 bits of GPIO for the MCF52274 (176 LQFP)
- Up to 55 bits of GPIO for the MCF52277 (196 MAPBGA)
- Bit manipulation supported via set/clear functions
- Various unused peripheral pins may be used as GPIO

2.6.27 System Debug Support

- Background debug mode (BDM) Revision B+
- Real time debug support, with four PC breakpoint registers and a pair of address breakpoint registers with optional data

2.6.28 JTAG Support

- JTAG part identification and part revision numbers

3 Developer Environment

The MCF5227*x* family of MCUs supports similar tools and third party developers as other Freescale ColdFire products, offering a widespread, established network of tools and software vendors.

The following development support will be available:

- Evaluation boards (EVBs)
- Compilers and debuggers
- Debug interfaces
- Initialization tool

The following software support will be available:

- Code examples
- Various module drivers (e.g., Ethernet, PCI, SPI, I^2C)
- Third party real-time operating systems (RTOS)

4 Revision History

Table 2 provides a revision history for this document.

Table 2. MCF52277PB Document Revision History

Rev. No.	Substantive Change(s)
0	Initial public revision
1	Removed general ADC features for touchscreen controller throughout

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