MCF5445*x* ColdFire® Microprocessor Product Brief

Supports MCF54450, MCF54451, MCF54452, MCF54453, MCF54454, & MCF54455

by: Microcontroller Solutions Group

The MCF5445*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 4 ColdFire microarchitecture. This product line is well suited for secure networked applications in factory automation, process control, and motion control. The rich feature set and flexibility make it attractive to many different applications in consumer and industrial markets.

All MCF5445*x* devices contain a Version 4 ColdFire core, 32-Kbyte internal SRAM, USB On-the-Go controllers, a 2-bank DDR/DDR2/mobile-DDR SDRAM controller, a 16-channel DMA controller, a serial boot facility, an SSI interface, and other serial interfaces. Optional peripherals include a PCI bus controller, ATA controller, Fast Ethernet controllers, and an encryption coprocessor.

This document provides an overview of the MCF5445*x* family and focuses on its diverse feature set. It covers the MCF54455 superset device, but is applicable to all derivative family members.

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1 Application Examples

The MCF5445*x* family is well suited for network-connected control applications that require a broad range of communication peripherals and high performance to enable competitive and cost-effective system solutions. As shown in the following examples, this microprocessor is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

1.1 Secure Home Network Data Storage

Figure 1 shows the MCF54455 used in a typical network storage application.

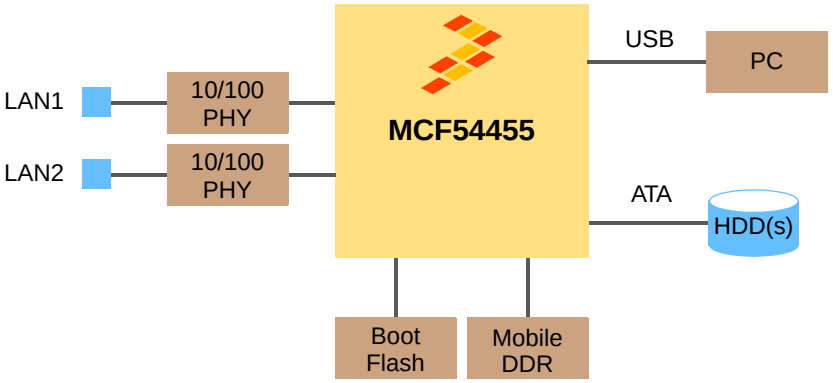


Figure 1. Secure Home Network Data Storage Example

1.2 Secure IP Camera

Figure 2 shows the MCF54455 used in a typical secure IP camera application.

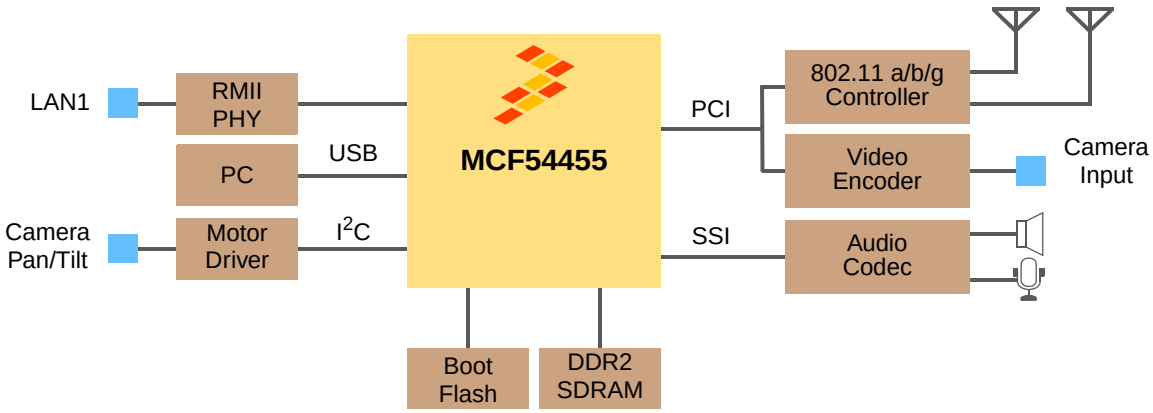


Figure 2. Wireless VoIP Telephone Example

2 Features

2.1 MCF5445*x* Family Comparison

The following table compares the various device derivatives available within the MCF5445*x* family.

Table 1. MCF5445*x* Family Configurations

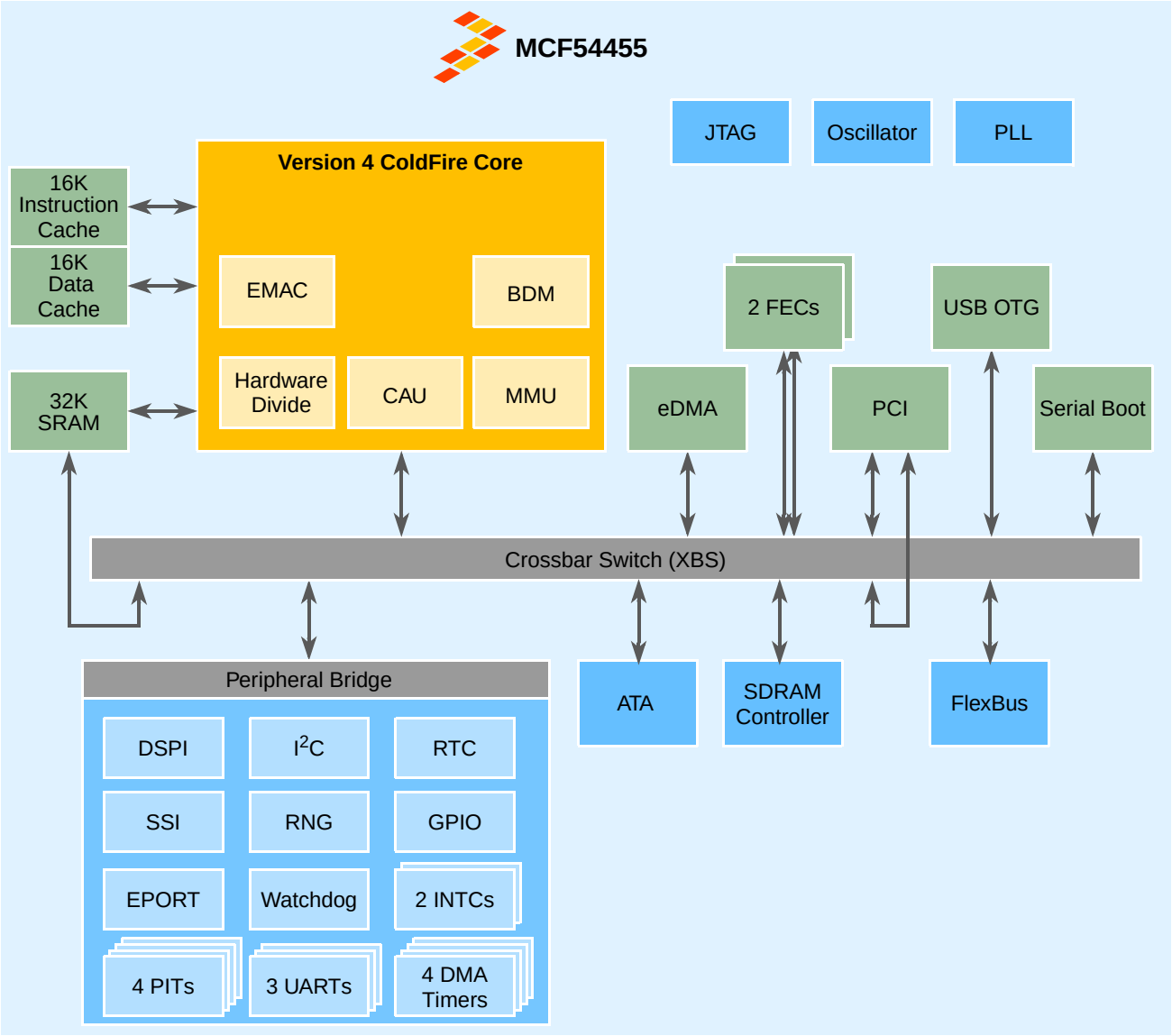
Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
ColdFire Version 4 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•
Core (System) Clock	up to 240 MHz		up to 266 MHz			
Peripheral Bus Clock (Core clock ÷ 2)	up to 120 MHz		up to 133 MHz			
External Bus Clock (Core clock ÷ 4)	up to 60 MHz		up to 66 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 370		up to 410			
Independent Data/Instruction Cache	16 Kbytes each					
Static RAM (SRAM)	32 Kbytes					
PCI Controller	—	—	•	•	•	•
Cryptography Acceleration Unit (CAU)	—	•	—	•	—	•
ATA Controller	—	—	—	—	•	•
DDR SDRAM Controller	•	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	•	•	•	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2	2	2
UARTs	3	3	3	3	3	3
I^2C	•	•	•	•	•	•
DSPI	•	•	•	•	•	•
Real Time Clock	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2	2

Table 1. MCF5445*x* Family Configurations (continued)

Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
16-channel Direct Memory Access (DMA)	•	•	•	•	•	•
General Purpose I/O (GPIO)	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•
Package	256 MAPBGA		360 TEPBGA			

2.2 Block Diagram

Figure 3 shows a top-level block diagram of the MCF54455 superset device.



LEGEND

ATA	– Advanced Technology Attachment Controller	**INTC**	– Interrupt controller
BDM	– Background debug module	**JTAG**	– Joint Test Action Group interface
CAU	– Cryptography acceleration unit	**MMU**	– Memory management unit
DSPI	– DMA serial peripheral interface	**PCI**	– Peripheral Component Interconnect
eDMA	– Enhanced direct memory access	**PIT**	– Programmable interrupt timers
EMAC	– Enchance multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random Number Generator
FEC	– Fast Ethernet controller	**RTC**	– Real time clock
GPIO	– General Purpose Input/Output	**SSI**	– Synchronous Serial Interface
I2C	– Inter-Intergrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Figure 3. MCF54455 Block Diagram

2.3 Operating Parameters

- 0ºC to 70ºC and –40ºC to 85ºC junction temperature devices are available
- 1.5V Core, 3.3V I/O, 1.8V/2.5V/3.3V external memory bus

2.4 Packages

Depending on device, the MCF5445*x* family is available in the following packages:

- 256-pin molded array process ball grid array (MAPBGA)
- 360-pin plastic ball grid array (TEPBGA)

2.5 Chip Level Features

- Version 4 ColdFire core with MMU and EMAC
- Up to 410 Dhrystone 2.1 MIPS @ 266 MHz
- 16 Kbytes instruction cache and 16 Kbytes data cache
- 32 Kbytes internal SRAM
- Support for booting from SPI-compatible flash, EEPROM, and FRAM devices
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 16 channel DMA controller
- 16-bit 133MHz DDR/mobile-DDR/DDR2 Controller
- USB 2.0 On-the-Go controller with ULPI support
- 32-bit PCI controller at 66 MHz
- ATA/ATAPI controller
- 2 10/100 Ethernet MACs
- Coprocessor for acceleration of the DES, 3DES, AES, MD5, and SHA-1 algorithms
- Random number generator
- Synchronous serial interface (SSI)
- 4 periodic interrupt timers (PIT)
- 4 32-bit timers with DMA support
- DMA supported serial peripheral interface (DSPI)
- 3 UARTs
- I^2C bus interface

2.6 Module-by-Module Feature List

The following is a brief summary of the functional blocks in the MCF54455 superset device. For more details refer to the *MCF54455 ColdFire Microprocessor Reference Manual* (MCF54455RM).

2.6.1 Version 4 ColdFire variable-length RISC processor

- Static operation
- 32-bit address and data path on-chip
- Maximum 266 MHz processor core, 133 MHz internal peripheral, and 66 MHz external FlexBus frequency
- Sixteen total general-purpose 32-bit registers data and address
- Enhanced multiply-accumulate unit (EMAC) for DSP and fast multiply operations
- Hardware divide execution unit supporting various 32-bit operations
- Implements the ColdFire Instruction Set Architecture, ISA_C
- Cryptography acceleration unit (CAU)
  - DES and AES block cipher engines
  - MD5, SHA-1, and HMAC hash accelerator

2.6.2 On-chip Memories

- 32 Kbyte dual-ported SRAM on CPU internal bus
  - Accessible to non-core bus masters (e.g. FEC, DMA, USB OTG, and PCI controllers) via the crossbar switch
- Non-blocking, independent 16 Kbyte data and instruction caches organized as 4-way set associative with 16 bytes per cache line and 1024 cache lines, supporting copy-back and write-through modes of operation

2.6.3 Phase Locked Loop (PLL)

- 16–40 MHz reference crystal
- Loss-of-lock detection

2.6.4 Power Management

- Fully static operation with processor sleep and whole chip stop modes
- Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Peripheral power management register to enable/disable clocks to most modules
- Software controlled disable of external clock input for low power consumption

2.6.5 Chip Configuration Module (CCM)

- System configuration during reset
- Bus monitor, abort monitor
- Configurable output pad drive strength control
- Unique part identification and part revision numbers

- Serial boot capability
  - Supports SPI-compatible EEPROM, flash, and FRAM
  - Configurable boot clock frequency

2.6.6 Reset Controller

- Separate reset in and reset out signals
- Six sources of reset: power-on reset (POR), external, software, watchdog timer, loss of lock, JTAG instruction
- Status flag indication of source of last reset

2.6.7 System Control Module

- Access control registers
- Core watchdog timer with a 2^n (where n = 8–31) clock cycle selectable timeout period
- Core fault reporting

2.6.8 Crossbar Switch

- Concurrent access from different masters to different slaves
- Slave arbitration attributes configured on a slave by slave basis
- Fixed or round-robin arbitration

2.6.9 Peripheral Component Interconnect (PCI) Bus

- Compatible with PCI 2.2 specification
- Supports up to 4 external PCI masters
- 32-bit target and intiator operation
- 33–66 MHz operation with PCI bus to internal bus divider ratios of 1:1, 1:2, 1:3, 2:3, and 1:4

2.6.10 Universal Serial Bus (USB) 2.0 On-The-Go (OTG) Controller

- Support for full speed (FS) and low speed (LS) via a serial interface or on-chip FS/LS transceiver
- Optional UTMI+ Low Pin Count Interface (ULPI) on some packages to support high speed (HS) transfers
- Uses 60 MHz reference clock based off of the system clock or from an external pin

2.6.11 DDR SDRAM Controller

- Supports a glueless interface to DDR, DDR2, and mobile/low-power DDR SDRAM devices
- Support for 16-bit fixed memory port width
- 16-byte critical word first burst transfer

- Up to 14 lines of row address, up to 11 column address lines (16-bit bus), 2 bits of bank address, and two pinned-out chip selects. The maximum row bits plus column bits equals 25.
- Supports up to 512 MByte of memory; minimum memory configuration of 8 MByte
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode

2.6.12 FlexBus (External Interface)

- Glueless connections to 16-, and 32-bit external memory devices (SRAM, flash, ROM, etc.)
- Support for independent primary and secondary wait states per chip select
- Programmable address setup and hold time with respect to chip-select assertion, per transfer direction
- Glueless interface to SRAM devices with or without byte strobe inputs
- Programmable wait state generator
- 32-bit external bidirectional data bus and 24-bit address bus
- Up to four chip selects available
- Byte/write enables (byte strobes)
- Ability to boot from external memories that are 8, 16, or 32 bits wide

2.6.13 Synchronous Serial Interface (SSI)

- Supports shared (synchronous) transmit and receive sections
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Gated clock mode operation requiring no frame sync
- Programmable data interface modes such as I^2S, LSB aligned, and MSB aligned
- Programmable word length up to 24 bits
- AC97 support

2.6.14 ATA Controller

- Compliant with ATA-6 specification
- Supports PIO modes 0, 1, 2, 3 and 4
- Supports multiword DMA modes 0, 1 and 2
- Supports ultra DMA modes 0, 1, 2, 3 and 4 with an internal bus clock of at least 50 Mhz
- Supports ultra DMA mode 5 with an internal bus clock of at least 80 Mhz
- 128 byte FIFO part of interface
- FIFO receive alarm, FIFO transmit alarm and FIFO end of transmission alarm to DMA unit
- Zero-wait cycles transfer between DMA bus and FIFO allows fast FIFO reading/writing

2.6.15 Fast Ethernet Media Access Controller (FEC MAC)

- 10/100 BaseT/TX capability, half duplex or full duplex
- On-chip transmit and receive FIFOs
- Built-in dedicated DMA controller
- Memory-based flexible descriptor rings
- Media independent interface (MII) to external transceiver (PHY)
- Separate RMII gasket to interface with RMII-compatible PHY

2.6.16 Random Number Generator (RNG)

- FIPS-140 compliant for randomness and non-determinism

2.6.17 Real Time Clock

- Full clock: days, hours, minutes, seconds
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
- Operation determined by reference input oscillator clock frequency and value programmed into user-accessible registers
- Ability to wake the processor from low-power modes (wait, doze, and stop) via the RTC interrupts

2.6.18 Software Watchdog Timer

- 16-bit down-counter which resets the device if not serviced

2.6.19 Programmable Interrupt Timers (PIT)

- Four programmable interrupt timers each with a 16-bit counter
- Configurable as a down counter or free-running counter

2.6.20 DMA Timers

- Four 32-bit timers with DMA and interrupt request trigger capability
- Input capture and reference compare modes

2.6.21 DMA Serial Peripheral Interface (DSPI)

- Full-duplex, three-wire synchronous transfer

- Up to five chip selects available
- Master and slave modes with programmable master bit-rates
- Up to 16 pre-programmed transfers

2.6.22 Universal Asynchronous Receiver Transmitters (UARTs)

- 16-bit divider for clock generation
- Interrupt control logic
- DMA support with separate transmit and receive requests
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to two stop bits in 1/16 increments
- Error-detection capabilities

2.6.23 I^2C Module

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- Fully compatible with industry-standard I^2C bus
- Master or slave modes support multiple masters
- Automatic interrupt generation with programmable level

2.6.24 Interrupt Controllers

- Two interrupt controllers, supporting up to 64 interrupt sources each, organized as seven programmable levels
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source plus a global mask-all capability
- Support for service routine software interrupt acknowledge (IACK) cycles
- Combinational path to provide wake-up from low power modes

2.6.25 Edge Port Module

- Each pin can be individually configured as low level sensistive interrupt pin or edge-detecting interrupt pin (rising, falling, or both)
- Exit stop mode via level-detect function

2.6.26 DMA Controller

- 16 fully programmable channels with 32-byte transfer control
- Data movement via dual-address transfers for 8-, 16-, 32- and 128-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes

- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration
- External request pins for up to 2 channels

2.6.27 General Purpose I/O interface

- Up to 93 bits of GPIO for the MCF54450 and MCF54451
- Up to 132 bits of GPIO for the MCF54452, MCF54453, MCF54454, and MCF54455
- Bit manipulation supported via set/clear functions
- Various unused peripheral pins may be used as GPIO

2.6.28 System Debug Support

- Background debug mode (BDM) Revision D+
- Real time debug support, with four PC breakpoint registers and a pair of address breakpoint registers with optional data

2.6.29 JTAG Support

- JTAG part identification and part revision numbers

3 Developer Environment

The MCF5445*x* family of MCUs supports similar tools and third party developers as other Freescale ColdFire products, offering a widespread, established network of tools and software vendors.

The following development support are available:

- Evaluation boards (EVBs)
- Compilers and debuggers
- JTAG interfaces
- Initialization tool

The following software support are available:

- Code examples
- Various module drivers (e.g., Ethernet, PCI, SPI, I^2C)
- Third party real-time operating systems (RTOS)

4 Revision History

Table 2 provides a revision history for this document.

Table 2. MCF54455PB Document Revision History

Rev. No.	Substantive Change(s)
1	Initial version.
2	In Family Configurations table, added PCI as feature on 256-pin devices. On these devices the PCI_AD bus is limited to 24-bits.
3	Rescinded previous change. The 256-pin devices do not contain the PCI bus controller.

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