MC1326

DUAL CHROMA DEMODULATOR

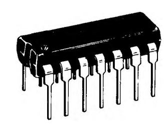
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

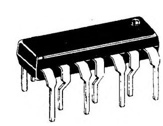
- Luminance Input Provided
- Good Chroma Sensitivity – 0.3 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing with Varying 3.58 MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 Vp-p typ
- Blanking Input Provided

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



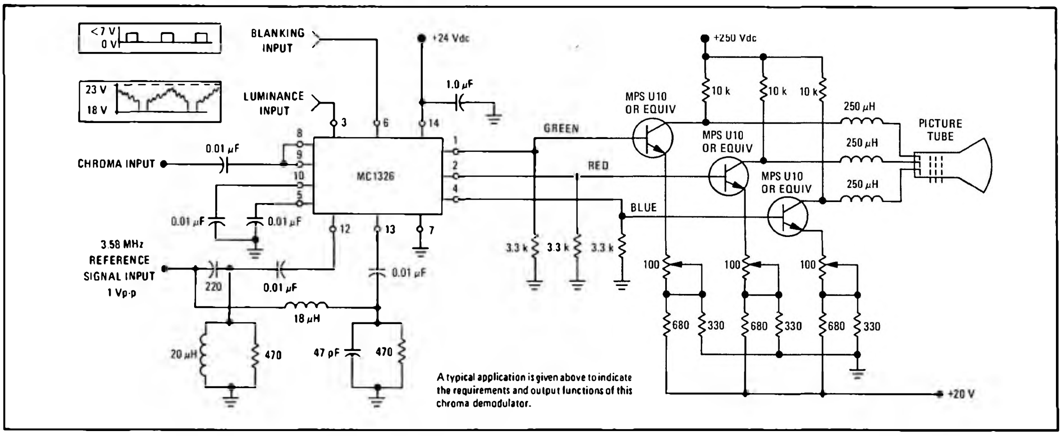
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

FIGURE 1 – MC1326 TYPICAL APPLICATION

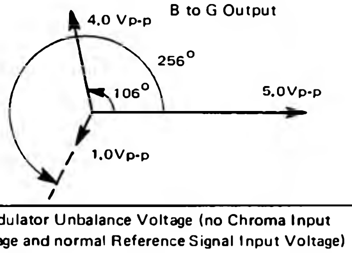


See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage See Figure 2	1, 2, 4	13	14.4	16	Vdc
Quiescent Input Current from Supply (Figure 2) (R_L = ∞) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (Reference Input Voltage = 1.0 Vp-p) See Note 1 and Figure 3	1, 2, 4	–	0.3	0.6	Vdc
Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 Vp-p, +25° to +65°C) See Note 1 and Figure 3	1, 2, 4	–	3.0	–	mV/°C

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
Blue Output Voltage Swing See Note 2 and Figure 4	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) See Note 3 and Figure 4	8	–	0.3	0.7	Vp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1, 2, 4	 – –	 0.95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) See Note 4 G Output R Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	Vp-p
Relative Output Phase (B Output = 5.0 Vp-p, Luminance Voltage = 23 V) B to R Output B to G Output 	 4, 2 4, 1	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1, 2, 4	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	4, 13	–	3	–	Degrees
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1, 2, 4	–	0.7	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	12, 13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12, 13	–	6.0	–	pF
Chroma Input Resistance	8, 9, 10	–	2.0	–	kΩ
Chroma Input Capacitance	8, 9, 10	–	2.0	–	pF

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p, all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the Blue Output Voltage = 5 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

TEST CIRCUITS

(V+ = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted)

FIGURE 2 – DC TEST CIRCUIT WITHOUT REFERENCE INPUT SIGNAL VOLTAGE (B-Y AND R-Y)
(For Testing Quiescent Current, DC Output Voltage, Difference Voltage)

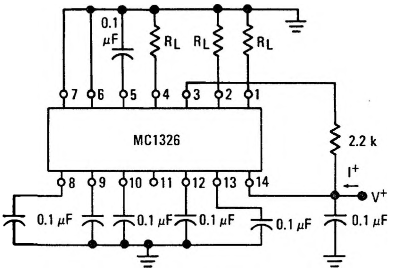


FIGURE 3 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

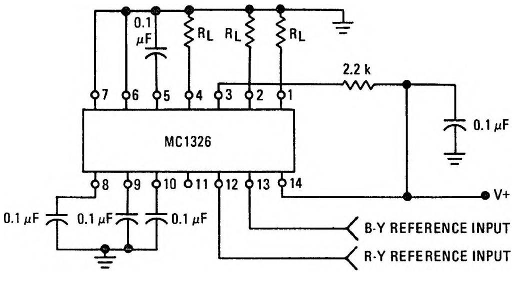
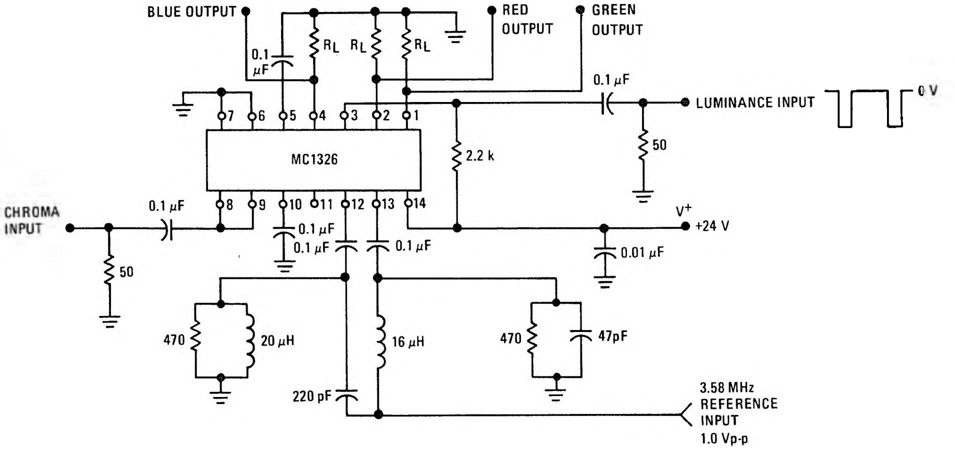
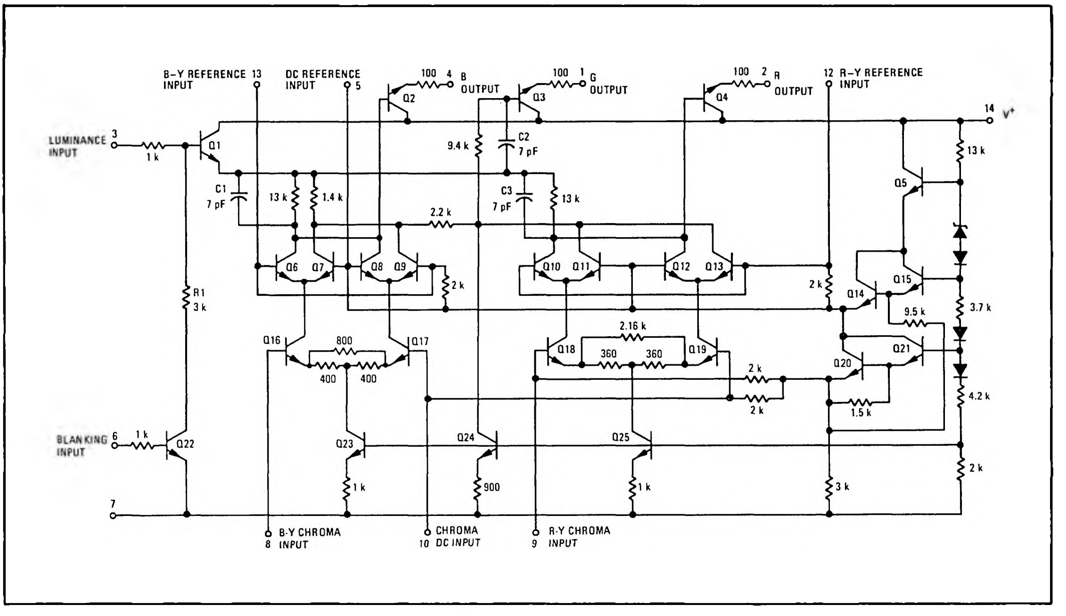


FIGURE 4 – DYNAMIC TEST CIRCUIT



MC1326 (continued)

FIGURE 5 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q16 and Q17, Q18 and Q19. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q6 and Q7, Q8 and Q9, Q10 and Q11, Q12 and Q13. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

While the detector section is almost identical to other available units, several excellent additional features are incorporated. Transistor Q1 is used as an emitter follower to which the collector load resistors of the detectors are returned. The collector impedances of the upper pair transistors are high compared with the collector load resistors, and any signal at the emitter of Q1 appears virtually unattenuated at the collectors of the upper pairs, and hence at the three detector output terminals. This feature may be used to mix the correct amount of the luminance portion of the color TV signal with the color difference signals produced by the detectors to give R-G-B outputs directly.

Capacitors C1, C2, and C3 compensate for most of the high frequency roll-off in the luminance signal. This is due to the collector capacitances of the detector transistors and the input capacitances of the emitter followers, Q2, Q3, Q4. Capacitors C1, C2, and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q2, Q3, Q4) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

If it is not required to mix the luminance signal via Q1, this transistor can be used for brightness control. If the base of Q1 is connected to a suitable variable dc voltage, this will vary the dc output levels of the three detected outputs accordingly and thereby vary the picture brightness level.

Blanking of the picture during line and frame flyback may be achieved by applying a positive-going blanking signal to the base of Q22. With an extra external resistor in series with the Q1 base of approximately 5 k ohms, when Q22 is turned on by the blanking pulse, the base of Q1 will be pulled negative by the current in R1, thus forcing all three detected outputs to go negative by the same amount. In a conventional solid-state receiver with a single video output stage driving the picture tube cathode, a negative-going signal at the base of the video output stage will blank the picture tube. When using the blanking input be certain the blanking pulse does not switch off the luminance input stage Q1 completely; this would turn off the collector supply for the demodulators and put the entire chroma demodulator out of lock at each blanking pulse.

Matrix for MC1326

$$\frac{\text{R-Y gain}}{\text{B-Y gain}} = 0.77$$

$$\text{-G-Y} = 0.11\ (\text{B-Y}) + 0.28\ (\text{R-Y})$$

For indicated requirements and output functions of the MC1326 chroma demodulator please refer to the typical application shown on the first page of this specification.

MC1326 (continued)

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted)

(Figures 6 through Figure 10 Reference Test Circuit of Figure 2)

FIGURE 6 – DC OUTPUT VOLTAGE

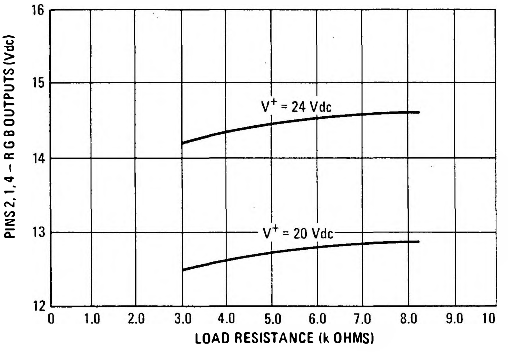


FIGURE 7 – POWER DISSIPATION

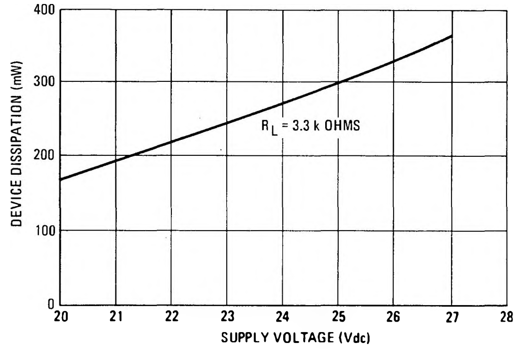


FIGURE 8 – DC OUTPUT VOLTAGE

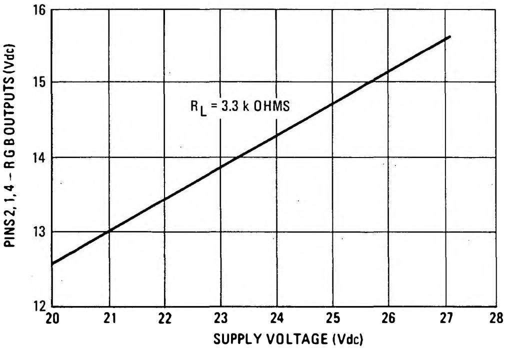


FIGURE 9 – POWER DISSIPATION

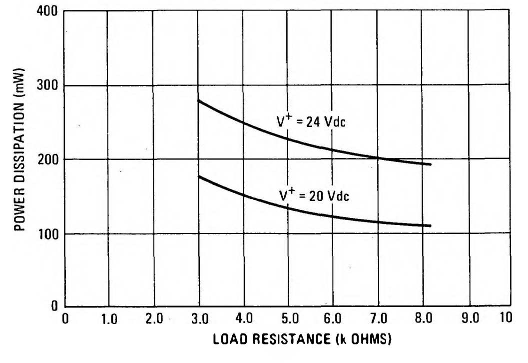


FIGURE 10 – DC OUTPUT VOLTAGE

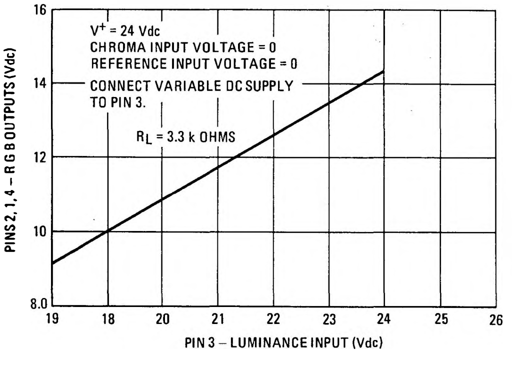
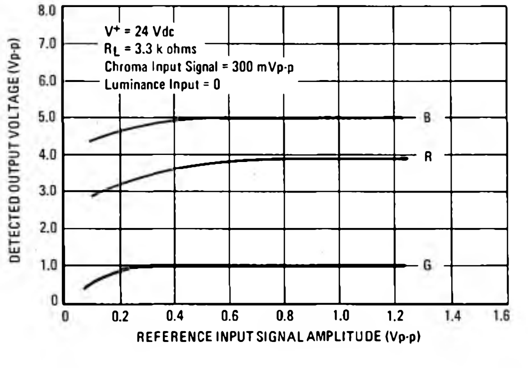


FIGURE 11 – DETECTED OUTPUT VOLTAGE
(Reference Test Circuit of Figure 4)



TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted)

(Figures 12 through Figure 17 Reference Test Circuit of Figure 4)

FIGURE 12 – OUTPUT VOLTAGE

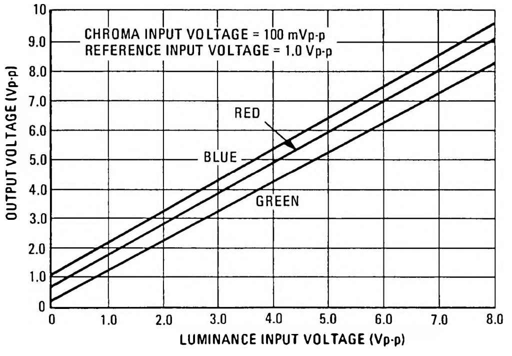


FIGURE 13 – GREEN OUTPUT

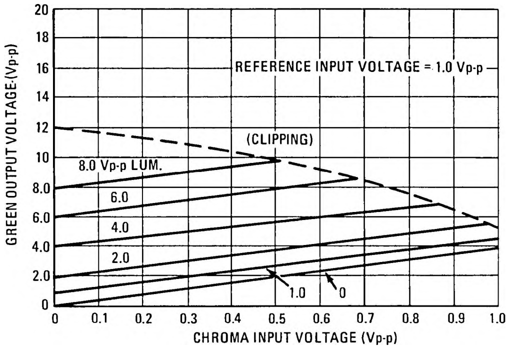


FIGURE 14 – RED OUTPUT

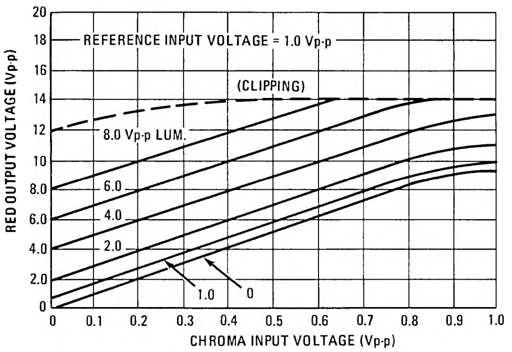


FIGURE 15 – BLUE OUTPUT

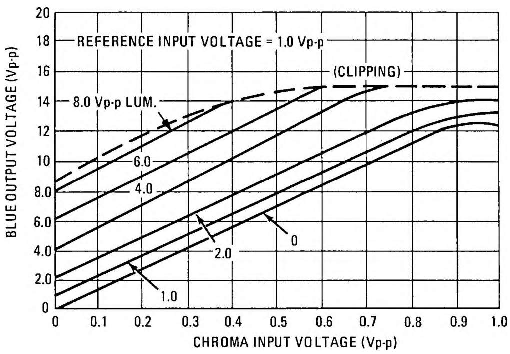


FIGURE 16 – LUMINANCE BANDWIDTH

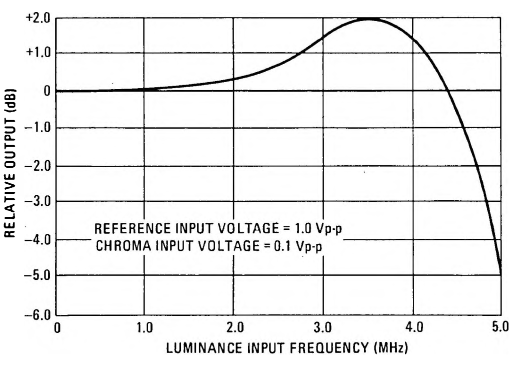


FIGURE 17 – CHROMA BANDWIDTH