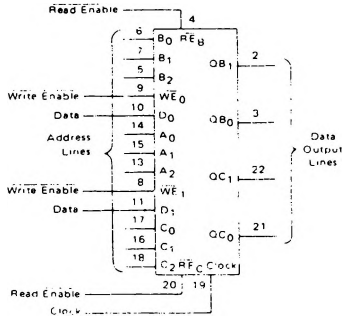


$t_{pd}$: Clock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
$\overline{\text{Read Enable}}$ to Data out = 3.5 ns
(Clock high, Addresses present)

$P_D$ = 610 mW typ/pkg

## 8 x 2 Multiport Register File (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE – The word to be written is selected by addresses $A_0$–$A_2$. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by $A_0$–$A_2$.

READ – When the clock is high any two words may be read out simultaneously, as selected by addresses $B_0$–$B_2$ and $C_0$–$C_2$, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates ($B_0$–$B_1$), ($C_0$–$C_1$).