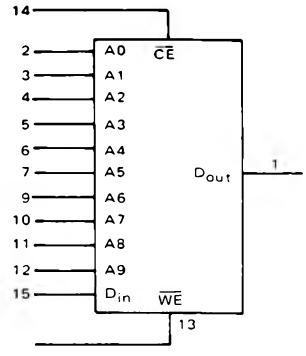

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø = Don't Care

Access Time: 22 ns typ
P_D = 510 mW/pkg. typ

1024-Bit Random Access Memory

The MCM10146 is a fully decoded 1024-bit Random Access Read/Write Memory organized as 1024 one bit words. Stored data is selected by means of a ten bit address, consisting of inputs A0 through A9.

The MCM10146 has an active-low chip enable input ($\overline{CE}$). The operating mode ($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is low and the data state present at the data input (pin 15) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 1).

Open emitter output permits full *wire-ORing* to data buses, with D_{out} low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.